5-2008

A Low Power Integrated Circuit for Implantable Biosensor Incorporating an On-Chip FSK Modulator

Taeho Oh

University of Tennessee - Knoxville

To the Graduate Council:

I am submitting herewith a thesis written by Taeho Oh entitled "A Low Power Integrated Circuit for Implantable Biosensor Incorporating an On-Chip FSK Modulator." I have examined the final electronic copy of this thesis for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Master of Science, with a major in Electrical Engineering.

Syed Kamrul Islam, Major Professor

We have read this thesis and recommend its acceptance:

Donald W. Bouldin, Jayne Wu

Accepted for the Council:
Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

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A LOW POWER INTEGRATED CIRCUIT FOR IMPLANTABLE BIOSENSOR INCORPORATING AN ON-CHIP FSK MODULATOR

A Thesis

Presented for the

Master of Science

Degree

The University of Tennessee, Knoxville

Taeho Oh

May 2008

Dedication

This thesis is dedicated to my mother and father,

Mrs. Seonbok Lee

and

Mr. Sangkyun Oh

For their guidance and direction in my life, as well as their support throughout my academic career

Acknowledgements

I would like to thank Dr. Syed Kamrul Islam for providing me an opportunity to pursue my Master's degree at the University of Tennessee and all the support and encouragement he has given me through out my graduate studies. I would also like to thank my thesis committee members, Dr. Donald W. Bouldin and Dr. Jayne Wu.

I am also thankful to MOSIS Educational Program (MEP) Research for supporting the fabrication of the chip.

I would also like to thank all the members of Analog VLSI and Devices Laboratory for their help in various aspects. Thanks to Mo Zhang, Chiahung Su and Mohammad Rafiqul Haider for their help with measurements and board design. I would like to give very special thanks to Wenchao Qu, and Pengfei Xi for their endless help with my design as well as my testing. Without these two people, I may not be able to complete my degree. Also, I would like to give special thanks to Mr. Bruce Coyne from Ametek Inc. He gave me a lot of advice when I designed the bandgap reference circuit and the voltage regulator

Finally, I would like to thank all the people that I know, and my parents, Mr. Oh, SangKyun, Mrs. Lee, SeonBok as well as my sister Dr. Oh, JiEun, my brother Oh, YoungHak.

Abstract

Medical care has been significantly improved in recent years due to tremendous technological advancement in the field of CMOS technology. Among those improvements, integrated circuit design and sensing techniques have brought to the doctors more flexibility and accuracy of examinations of their patients. For example, a diabetic patient needs to visit a hospital on a regular basis for the examination and proper treatment. However, with the tremendous advancement in electronic technology, a patient can soon monitor his or her own blood glucose level at home or at office with an implantable sensor which can also trigger insulin pump attached to the body. The insulin delivery system can be precisely controlled by the electronics embedded in the implantable device.

In this thesis, a low power integrated circuit for the implantable biosensor incorporating an on-chip FSK modulator is presented. This design has been fabricated using AMI 0.5-μm CMOS process available through MOSIS. The simulation and test results are also presented to verify its operation

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Chapter 1

INTRODUCTION

1.1 Biosensor

The advancement in integrated circuit technology and sensing techniques in the last few decades have made the widespread use of sensor techniques possible in modern biomedical applications[1]. The high degree of miniaturization now possible for the classical measurement techniques has led to the realization of complex analytical systems, including sensors that are known as “BioChemLab-on-a-Chip”. In addition, the recent improvement in the fabrication capabilities of microelectronics industries down to the micro- and nano-scales, and widely available and inexpensive systems have made the development of a variety of novel biomedical sensors possible[2]. Such improvement in technologies and adoptability in various applications have increased the demand for the growing use of personal monitoring devices such as glucose sensors for diabetics, sensors for HIV detection, blood pressure sensor, etc[2]. Recent advancements in biomedical sensors allow one to use these devices in personal medical care and can be easily modified for an individual patient’s needs. In near future, such improvements in biomedical sensors will give the patients better treatment options according to their biological rhythms and health conditions. This will also provide more information about the condition of the individual patients so that the doctors can provide better medical care for each according to the individual needs. For instance, the doctors can prescribe a medicine more accurately based on the data from the sensors in order to maximize the healing time and minimize its side effects. Also, the biomedical sensors will allow a doctor to communicate with the patient from a remote location using a variety of systems such as personal computers and internet.

1.2 Powering of the Implantable Biosensor

A biomedical sensor is a device that converts the biochemically or biologically produced sensing information into an electrical signal. The use of submicron devices for medical applications in highly desirable because of following reasons[3]:

- Small size and weight of the implants, options for minimal invasive surgery and continuous patient monitoring.
- Low power consumption for implants, continuous monitoring and the availability of inductively-coupled power supply via telemetry.
- Integration of systems for low signal-to-noise ratio, increased reliability, and telemetric options.
- Low-cost of production resulting in cost reduction in health care and disposable devices for reduced risk of infection.

In order to design a practical and a successful implantable precision biomedical sensor, a designer should solve following problems first[4]:

- A means for supplying electrical power to the implanted unit that is non-invasive, reliable, long lasting, efficient and inexpensive.
- A means for data communication between the implanted unit and an external unit that is robust, reliable and provides measured data in real time.

Batteries can be used as an alternative approach for delivering power to the implantable systems. However, there are also problems associated with using batteries as follows:

- Some applications require more ampere-hours than an implantable battery can provide, which necessitates frequent re-implantation or recharging of the battery.
- Batteries can be considerably large and can potentially leak causing hazard to body tissues.

Like a battery, a wired data communication system is not a good choice for the implantable systems for the reasons similar to the ones discussed above.

Fig.1.1 shows an example of telemetry system of an implantable biosensor[5]. To prevent problems induced by batteries or any wired data communication, wireless system is the best solution until now[6]. The advantages using telemetry systems are:

- Reduction of implanted area
- Suppression of immune response

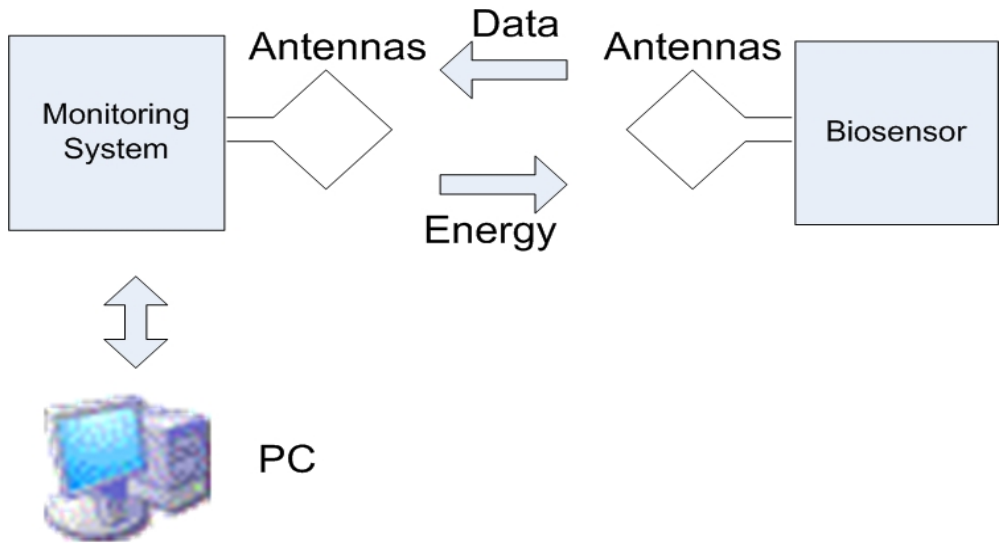


Fig. 1.1 Block diagram of the monitoring system[5].

- Increase of portability

However, the telemetry system has the following drawbacks:

- Limitation of available power.
- The size of the implanted coil.
- Attenuation of signal through the human skin.

In spite of the above disadvantages, the wireless powering and wireless data communication system are preferred by most biomedical sensor designers primarily because of their long-term service abilities, ease of operation etc.

1.3 System Overview

There are two main concerns that a designer should have: (1) long term bio-compatibility, and (2) power management. Both of these facts are important since the sensor will be implanted into the human body or on the skin and there is a size limitation of possible implanted area. In addition, there exists a limitation on power consumption. Using CMOS technology to design microelectronic circuit for biomedical sensor is one of the best choices because of its small size as well as low power consumption. The power and the data from the sensor will be transferred through the wireless system via inductive link. Therefore, telemetry system will not only improve the system life but also will make sure a secured transmission of data In this thesis, biomedical sensor system design with frequency shift keying (FSK) modulated implantable biosensor is presented.

1.4 Scope of Thesis

Chapter 1 will describe the back ground of Biosensor, and the usual technique to power up the biosensor.

Chapter 2 will present the ASK modulation techniques beginning with system level design. In the later part of the chapter test chip result of a previously designed ASK modulation circuit will be presented.

Chapter 3 will describe the FSK modulation schemes. In the beginning of the chapter a comparative analysis of the FSK modulation and ASK modulation schemes will be presented, followed by a discussion on the decision to choose FSK scheme for the implantable wireless biosensor application. In addition, a detailed description of circuits that has been used in this design will be presented.

Chapter 4 will mainly discuss the layout, simulation results as well as test results of the complete FSK modulation circuit.

Chapter 2

A LOW POWER INTEGRATED CIRCUIT FOR IMPLANTABLE SENSOR: ASK MODULATION SCHEME

2.1 Complete System Design Overview

Previously, an implantable biosensor with ASK modulator has been developed. The block diagram of this system is shown in Fig. 2.1[7]. This design has been implemented in TSMC 0.35-μm 2-poly-4metal CMOS process available through MOSIS (MOS Implementation Service). In Fig. 2.2, the unregulated voltage of 2.5V is from an external power source which is derived from a wireless link. Since this system will be implanted inside the human body or on the skin, the power consumption of chip will be limited by the availability of the appropriate power supply.

A conventional power source such as a battery can not be implanted with sensor because of various reasons as explained in previous chapter. As a result, powering by wireless link will be a very practical alternative. Wireless power source as well as the on-chip wireless transmitter are the two key design requirements of the implantable biosensor which provide the capability of *in vivo* recording and transmission of signals, elimination of long connecting wires/cables and suppression of the immune responses or infections.

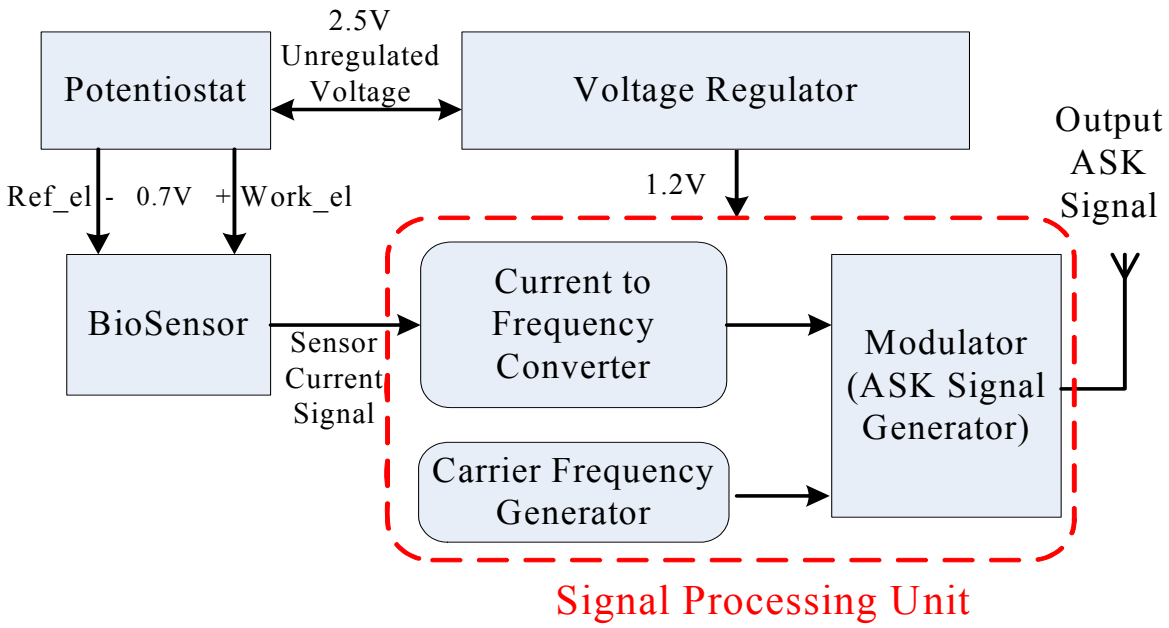


Fig. 2.1 Block diagram of the implantable sensor with ASK modulator

2.2 The Potentiostat Design

The potentiostat as shown in Fig. 2.3 is one of the key functional building blocks of this design as it provides appropriate bias voltage for the proper operation of the electrochemical sensor. The electrochemical biosensor produces a sensor current as long as the *work_electrode* (*Work_el*) and the *reference_electrode (Ref_el*) maintain a fixed voltage of 0.7V. For the operation of the particular sensor as potential difference between the *work_electrode* and the *reference_electrode* of 0.7V is desired. This results in a current through the *collection_electrode* (*Collect_el*) which is proportional to the target analytes in the chemical solution and is fed to the on-chip signal processing unit[7].

The operation of the potentiostat circuit can be explained as follows. U1 through U4 are a set of operational amplifiers, which are the basic building blocks of the potentiostat. U1 and U2 work as buffers, U3 works as a unity gain differential amplifier and finally U4 works as an error amplifier. Voltage Regulator sustains a stable reference voltage of 1.2 V which is reduced to 0.7 V by a voltage divider at the non-inverting terminal of the error amplifier. The output of the error amplifier is fed back to the *work_electrode* to compensate for any deviation from 0.7V voltage difference between the *work_electrode* and the *reference_electrode*. The operation of the potentiostat can be explained by the following equations derived by applying Kirchoff's current law (KCL) at the inverting terminal of U3[7].

$$V_{ref\_el} - \frac{V_{work\_el}}{2} = \frac{V_{work\_el}}{2} - 0.7$$
$$\therefore V_{work\_el} - V_{ref\_el} = 0.7 \qquad (2.1)$$

Where, $V_{reference}$ and $V_{work\_electrode}$ are the potential of reference and work electrode. Also, all amplifiers are assumed to be as ideal amplifiers[7].

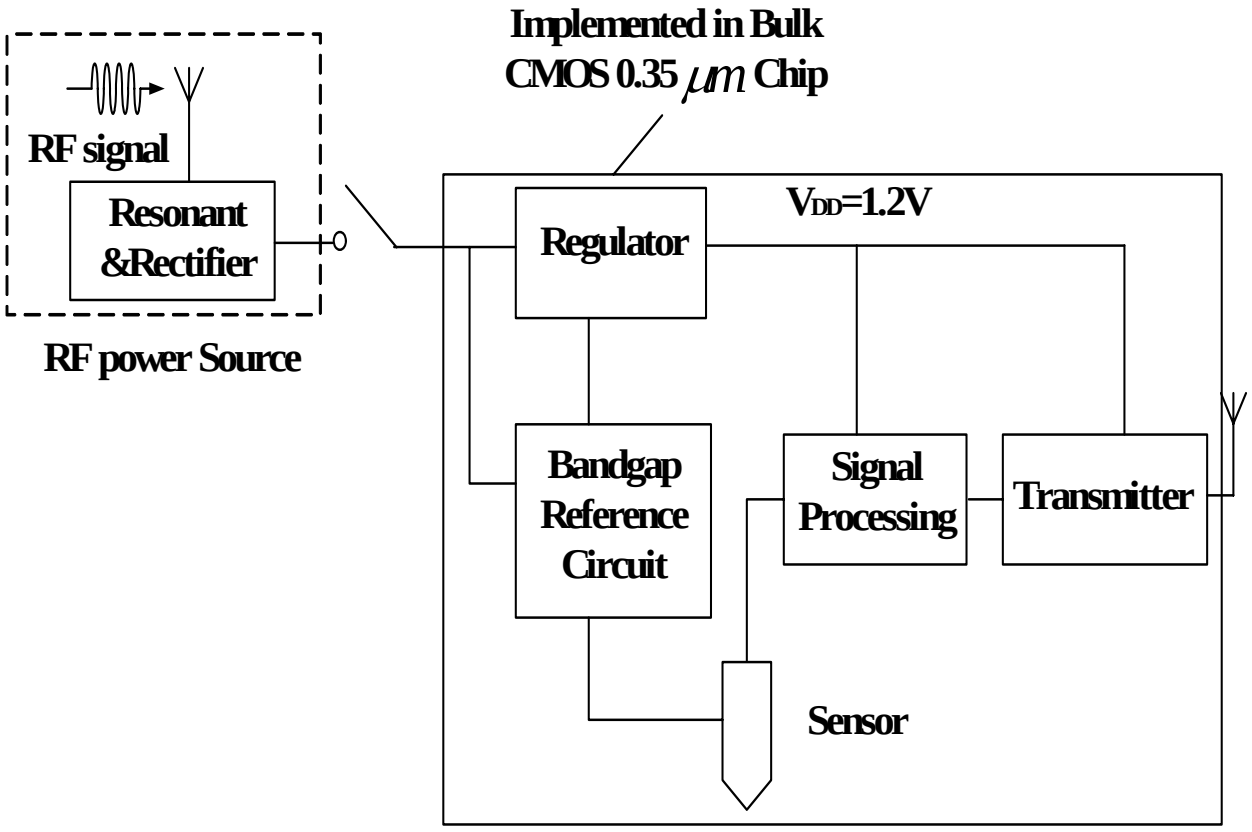


Fig.2.2 Block diagram of the sensor system with off-chip wireless power source and on-chip transmitter

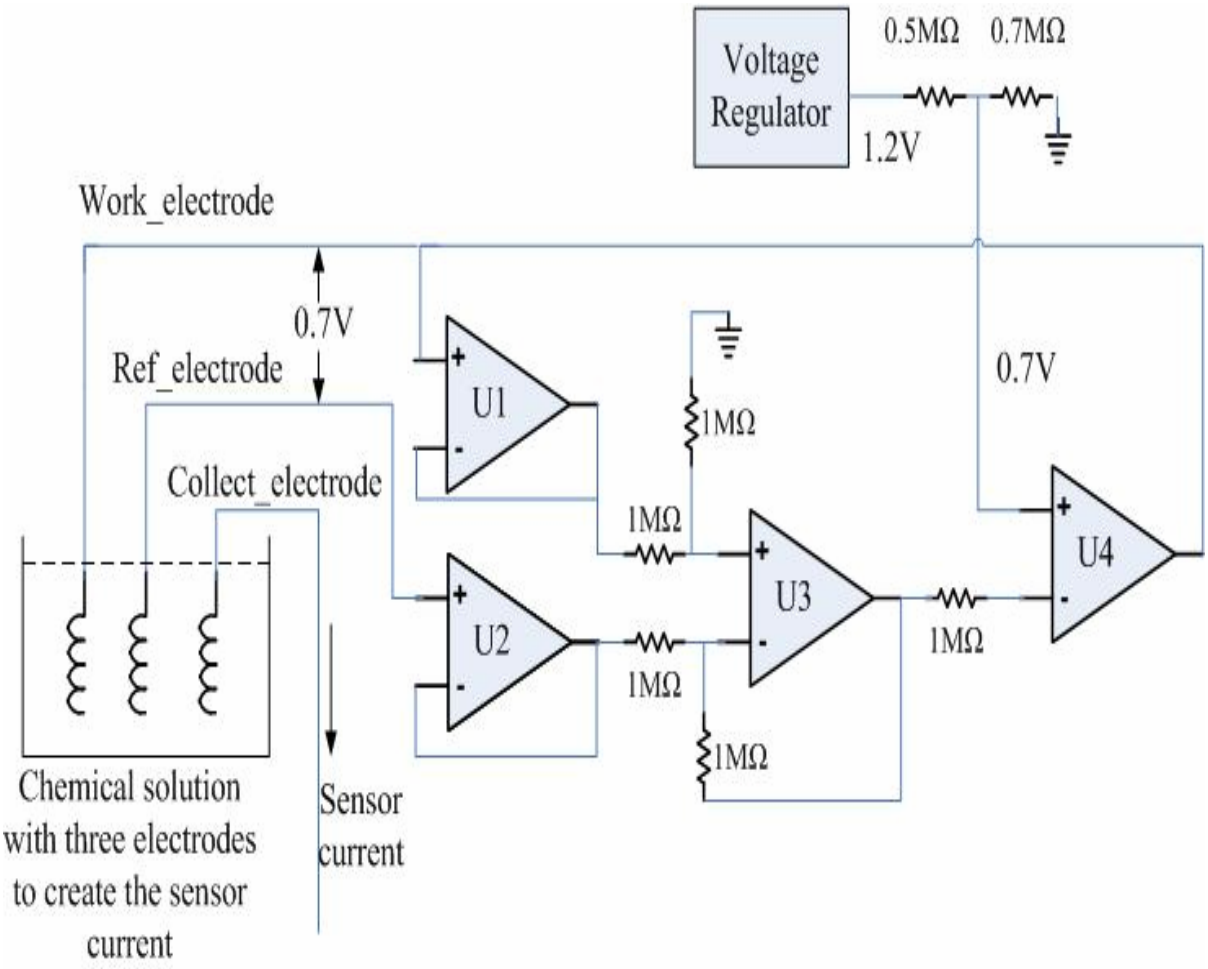


Fig.2.3 Block diagram for the potentiostat circuit

2.3 The Voltage Regulator Design

A low-dropout voltage regulator topology has been used to supply a stable voltage received from the wireless power source and to make sure that the data transmitted out is reliable as well. Fig. 2.4 shows the conventional schematic of a low-voltage, a low-dropout voltage regulator[8]. The voltage regulator is made up of a bandgap voltage reference circuit, an operational transconductance amplifier, and a PMOS transistor with a large W/L ratio. A large PMOS transistor is used to provide adequate amount of current that will be consumed by the signal processing block.

This voltage regulator produces a reliable 1.2V supply voltage for the entire signal processing block. The most important component in the design of this voltage regulator is an operational transconductance amplifier (OTA). To make this regulator work properly with a low supply voltage on the order of 1V, the topology chosen for the operational transconductance amplifier consists of two input differential pairs[8].

In this topology, both the PMOS and the NMOS differential input pairs at the input stage are used to provide a rail-to-rail input swing. To achieve a high output resistance, a cascade output stage topology has been implemented as an output stage. To make sure that the OTA is working at a low supply voltage, the biasing network as shown in Fig. 2.5 has been implemented. Because of the small value of transconductance of the input stage, the bandwidth of OTA will be reduced.

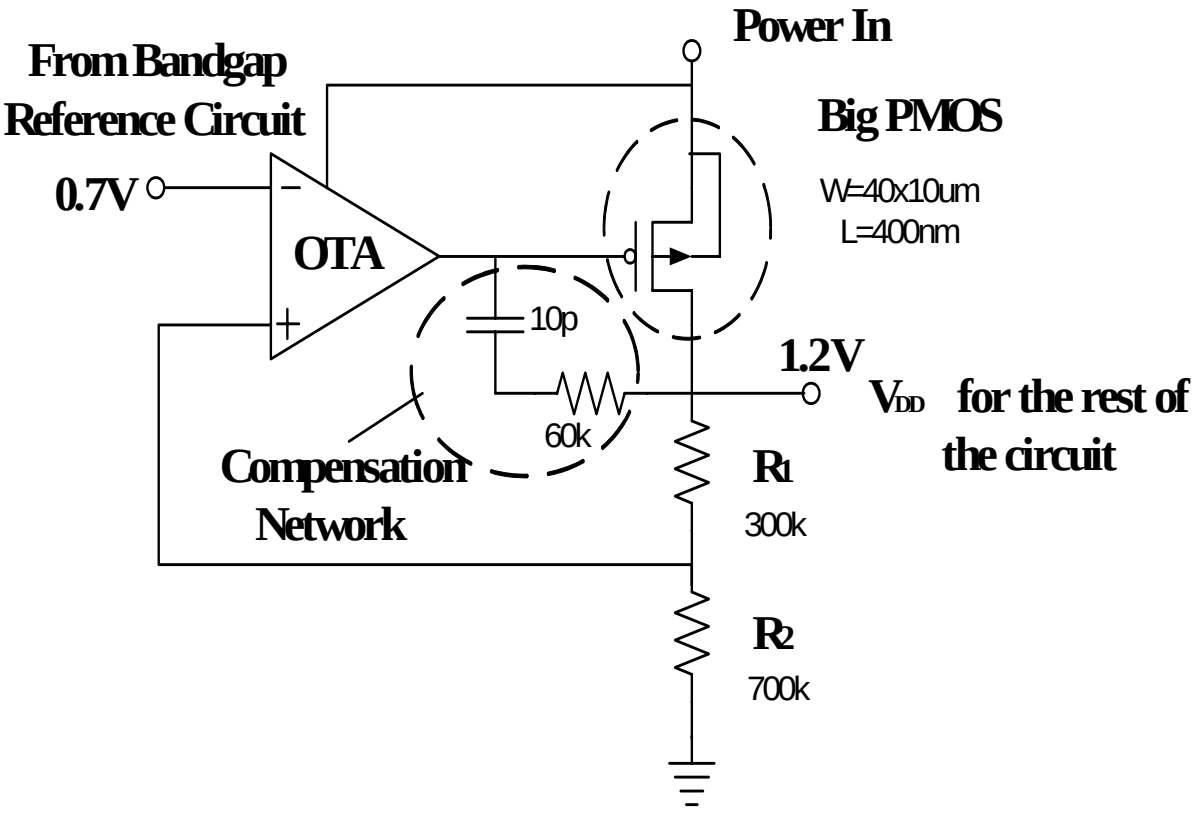


Fig.2.4 On-Chip voltage regulator circuit

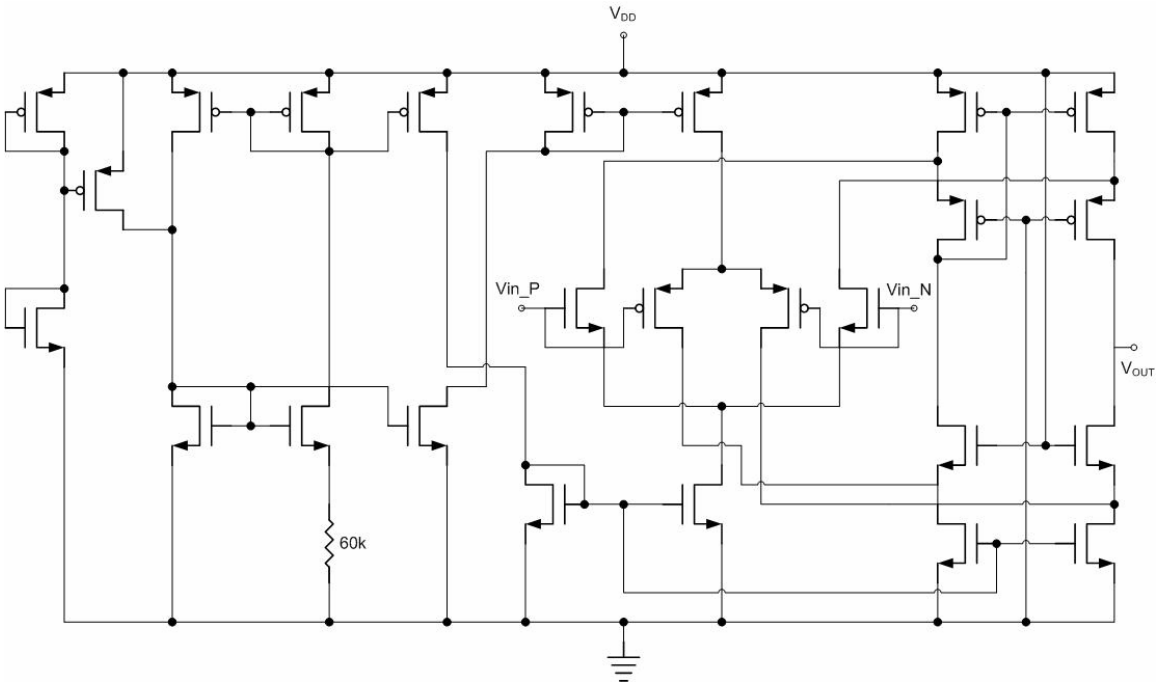


Fig.2.5 Detailed schematic of the OTA used in the regulator circuit

Furthermore, the low supply voltage will limit the overall performance of OTA. The large PMOS transistor provides a negative feedback, which pushes the inverting input voltage of the amplifier to be equal to its non-inverting input. As a result, the output supply voltage for the entire signal processing block from voltage regulator will be the same as the bandgap reference output voltage of 1V, which is stable with external supply voltage variations as well as a wide temperature variations[8].

2.4 The Bandgap Reference Design

The bandgap reference voltage circuit has an operational amplifier, two PMOS transistors, two large on-chip resistors, two bipolar junction transistors, and a start-up circuit. Fig. 2.6 represents the block diagram of a bandgap voltage reference circuit[7]. A bandgap reference voltage circuit is one of the essential components of most of modern day circuit designs and is usually used to supply a stable reference voltage to the circuit that might be compared with other voltages. In the ASK modulation circuit, a bandgap voltage reference has been also used to provide a stable reference voltage for the voltage regulator, a stable current for the OTA, the potentiostat, and the voltage regulator over certain temperature and power supply variations.

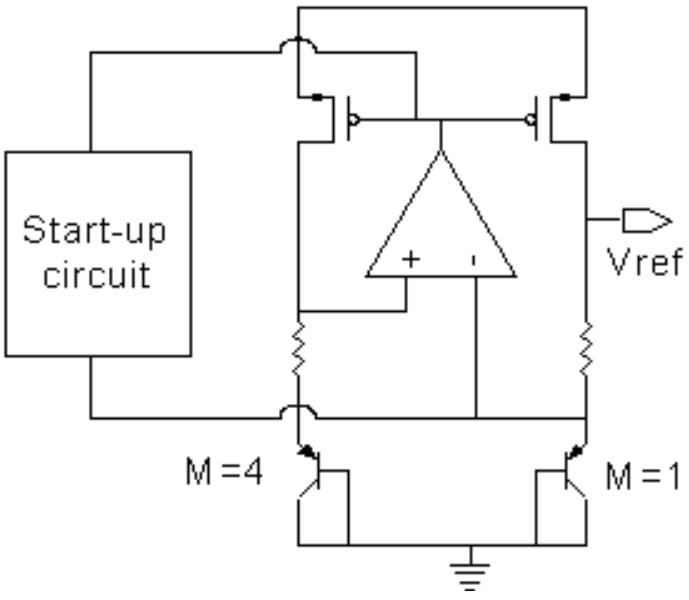


Fig.2.6 Block diagram of a bandgap voltage reference circuit

2.5 The Signal Processing Block-ASK Modulation

Table 2.1 shows the typical modulation techniques used in a modern communication system design[4].

- FSK – Frequency Shift Keying
- OOK – On Off Keying
- ASK – Amplitude Shift Keying
- BPSK – Binary Phase Shift Keying
- PWM – Pulse Width Modulation
- Packet Detect

The first three are the most popular modulation techniques.

On the other hand, for backward data communication topology, the techniques used are followings[4]:

- LSK – Load Shift Keying (also known as load modulation)
- ASK - Amplitude Shift Keying
- PWM – Pulse Width Modulation
- DBPSK – Differential Binary Phase Shift Keying
- Burst of RF energy,

Among these, LSK is the most commonly used in communication circuits. In Table 2.1, a comparison between various types of digital modulation schemes commonly used in communication electronics is presented. ASK has been chosen as the modulation scheme for backward communication due to the simplicity of design, requirement of small chip area, and easy implementation despite its inherent disadvantages as listed in Table 2.1[4].

Table 2.1 Comparison of Modulations Schemes

ASK	OOK	LSK	FSK	BPSK/DBPSK
• Noncoherent • Simple • Inexpensive • Poor performance, as it is heavily affected by noise and interference • Low power efficiency • Should only be considered when the signal-to-noise ratio is very high	• Non-coherent • Simple • A special form of ASK, where no line spectra are produced due to 100% modulation • Despite of reduced transmitter power than ASK, still inefficient in using power • Inferior error performance as ASK	• Simple • Does not require a carrier • Utilizes the property of an inductive link that the load impedance seen by the secondary coil reflects back to the primary side and becomes a part of the primary coil's load • By modulating the load of the implanted circuit and detecting it by the voltage variations across the external coil, backward data transmission is achieved • The performance	• Can be noncoherent or coherent • Constant or nearly constant amplitude, and insensitive to amplitude variations • Better noise performance than amplitude modulation schemes • Moderate bandwidth efficiency • High power efficiency • Simple, low-cost implement-ation possible	• BPSK is coherent, while DBPSK can be noncoherent as it compares the phase in one interval to the phase in the previous interval. • BPSK generally shows better error performance than ASK and FSK; but the error probabilities are double with DBPSK. • Bandwidth efficiency is similar to FSK. • Low power efficiency

Table 2.1 Comparison of Modulations Schemes continues

ASK	OOK	LSK	FSK	BPSK/DBPSK
		of this scheme highly depends on the coupling insensitivity of the link, and hence does not offer a robust communication choice		• Usually implementa-tion is complex and more costly than other techniques

Fig. 2.7 represents the schematic of the signal processing unit. This circuit produces an ASK signal, which can be demodulated and reproduced with a conventional commercial radio[7]**.** This block can accommodate any kind of implantable electrochemical sensor, which can produce certain level of current in response to the target analyte. The current level that is used in this block is in the range of 0.2μA to 2μA. For the input part of the circuit, a current mirror is used (N1 and N2). The diode-connected NMOS (N1) in the current mirror stabilizes the voltage at the terminal connected to the potentiostat to be about the threshold voltage (V_{th}) of the NMOS, which is around 0.5V. The mirror current charges the integrating capacitor to the supply voltage resulting in a decreasing voltage at the input of the Schmitt trigger. At the moment, the voltage goes below the threshold voltage of the Schmitt trigger the PMOS switch turns on and discharges the capacitor to start the new cycle. The charging rate of the capacitor is controlled by the mirror current which is in turn proportional to the sensor current. Thus, the oscillation frequency is directly proportional to the sensor current level.

The entire circuit is designed to consume very small amount of power and to work with a very low supply voltage. A voltage regulator is designed to supply a stable V_{DD} (approximately 1.25V) for the signal processing block[7]. This is a subtlety to generate a stable frequency for both the carrier frequency generator and the signal processing block for a given electrochemical sensor current.

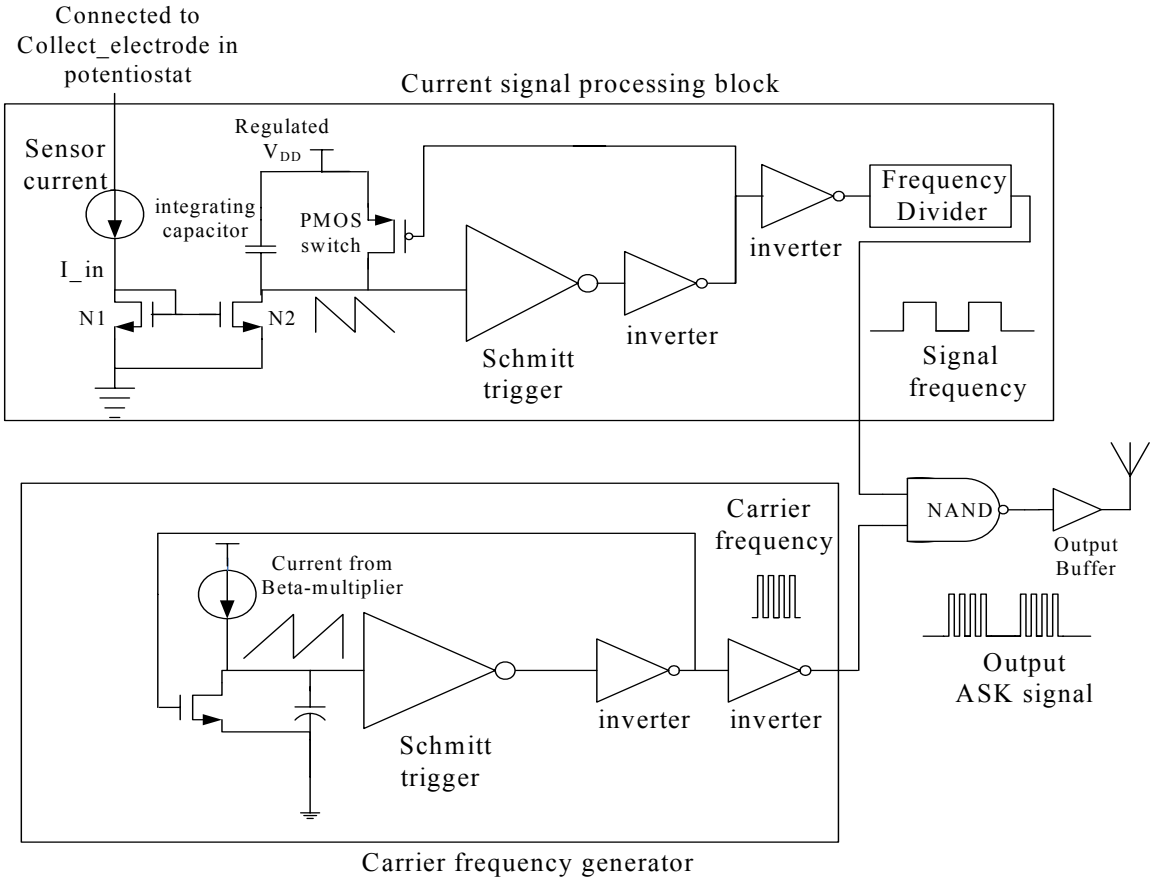


Fig. 2.7 Block diagram of signal processing unit

2.6 Test Results of ASK Modulation

Fig. 2.8 shows the test result for the implantable biosensor with ASK modulation circuit[7]. Test results demonstrate the proper operation of the ASK modulator circuit and compares well with the simulation results

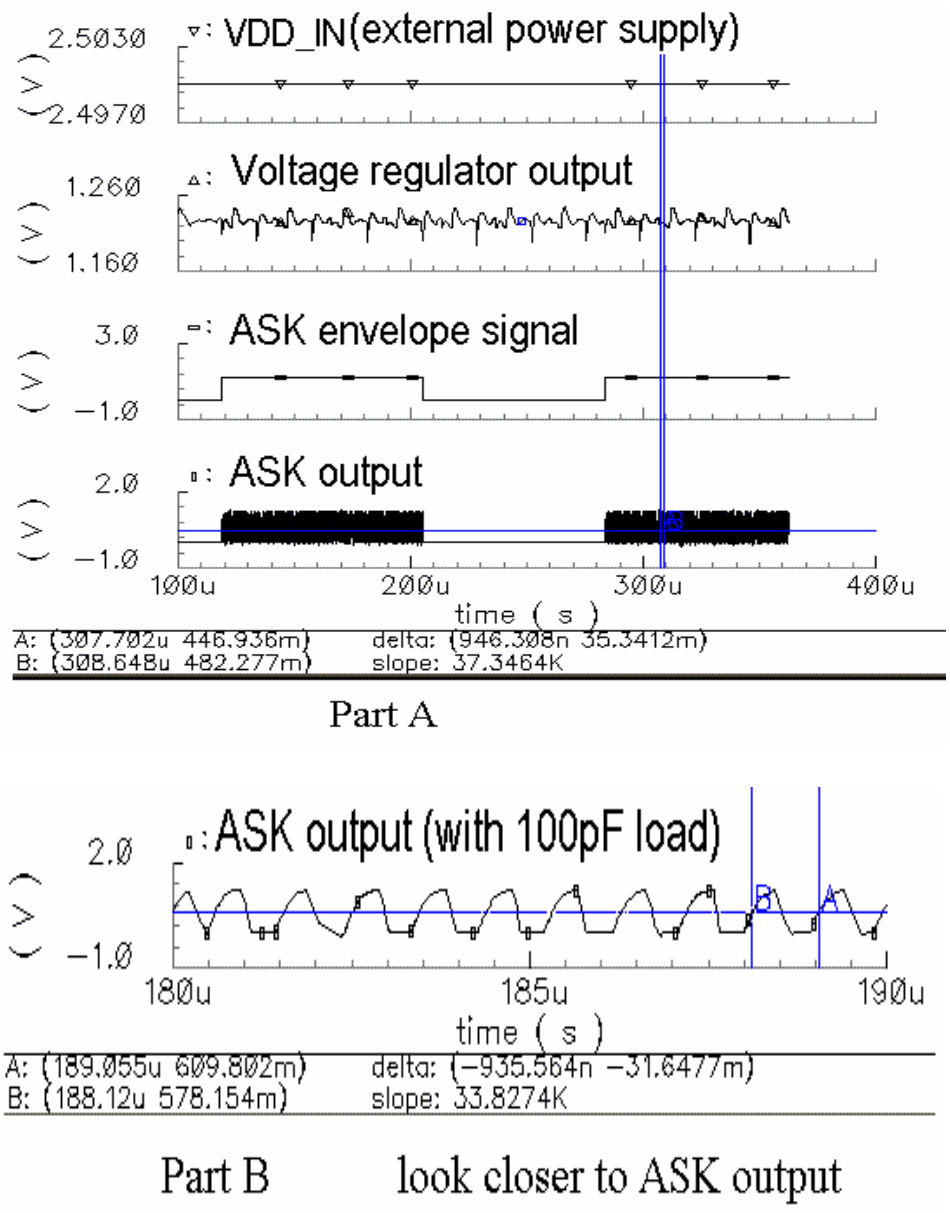


Fig. 2.8 Test results of the complete system

Chapter 3

A LOW POWER INTEGRATED CIRCUIT FOR IMPLANTABLE SENSOR: FSK MODULATION SCHEME

3.1 Signal Processing Block- FSK Signal Generator

3.1.1 Amplitude Shift Keying versus Frequency Shift Keying Modulation

Using an inductive link between the two magnetically coupled coils is now one of the most widely used methods to couple power and data between implanted biosensor and outside data receiver[6]. Using telemetry system to send power and receive the data from an external device to a biosensor is effective because of its small required area to be implanted as well as its minimized side effect or suppression of the immune response. Implanting battery or wired power delivering or receiving data will increase the required implant area, cost, and can result in the increased the chances of a number of biological problems.

Among the various modulation techniques as listed in Table 2.1, ASK and FSK are considered because of their relatively simple way of design and low cost of manufacturing compared to other digital communication techniques[4, 9]. Amplitude Shift Keying (ASK) is one basic method that a designer can choose. The main advantages of ASK are its fairly low cost and simplicity o implementation. However, ASK modulation technique has a low power efficiency and high error rate during the transmission.

On the other hand, an FSK modulation circuit is relatively simple to implement but unlike ASK, FSK has better performance over the transmission error since it uses the frequency modulation technique. An FSK signal modulates the data by using two different carrier signals: high-, and low-carrier. Because of the above reasons, an FSK modulation scheme has been chosen in this design.

3.1.2 Designing Data Frequency and Carrier Frequency Generator

From the system design requirements, the data should be generated from the current that is generated by the biosensor in response to the presence of an analyte. Potentiostats are used to set bias voltages for the proper operation of the sensor. The potentiostat consists of three pins: w*ork_electrode*, *reference_electrode*, and *collect_electrode*. If the potential difference between *work_electrode* and *reference_electrode* is maintained at 0.7V, the *collect_electrode* produces the current, which is in the range of 0.2uA to 2uA. This current is then converted to a data signal of a certain frequency by the signal processing electronics[7].

The circuit topology used to produce the data frequency is shown in Fig. 3.1[10]. M1 and M2 are simple NMOS current mirrors, and M3 to M6 are also simple PMOS current mirrors. The data frequency generation circuit can be redrawn as shown in Fig. 3.2, which represents a simple form of a ring oscillator. A ring oscillator is a positive feedback system. To make sure that the system works as an oscillator, the Barkhausen criteria should be satisfied with a total phase shift of 360^0 and a loop gain should be equal to a unity[11]. Since a single-stage inverter has only one pole, the phase shift of a single-stage inverter has 90^0, which is not a sufficient condition for oscillation. To get the required phase shift, several inverters should be cascaded

and the number of cascaded stages should be an odd number. To make sure that the oscillator has sufficient loop gain, and the required phase shift for oscillation, Fig.3.2 can be used to analyze the design of a three-stage ring oscillator[11]. Each stage of the ring oscillator has one single pole with loop gain equal to $-G_mR_o$, the transfer function can be written as:

$$H(j\omega_{OSC})= \left(\frac{-G_m R_o}{1+ j\varpi_{OSC} R_o C_o} \right)^3$$

$$\tan^{-1}(\omega_{OSC}R_oC_o) = 60^0 \qquad (3.1)$$

$$\therefore G_mR_o = 2$$

If the above criteria are satisfied, the ring oscillator can oscillate, and the output waveform should be a square wave. This ring oscillator is also called as voltage controlled oscillator (VCO) since its frequency is controlled by the input voltage. However, the difference between Fig. 3.1 and Fig. 3.2 is the source, which controls the frequency. Instead of using voltage source to control the frequency, a generator used in Fig. 3.1 employs the current to control the frequency, which also, calls as current controlled oscillator (CCO)[10]. A ring oscillator consists of a number of delay stages. If N gain stages (Inverter Stage) are cascaded with an odd number of inverters in a feedback loop, the circuit will oscillate with a period equal to $2NT_d$, where T_d is the delay for each stage. Below equation the frequency of oscillation[12].

$$f_{OSC} = \frac{1}{2NT_d} \qquad (3.2)$$

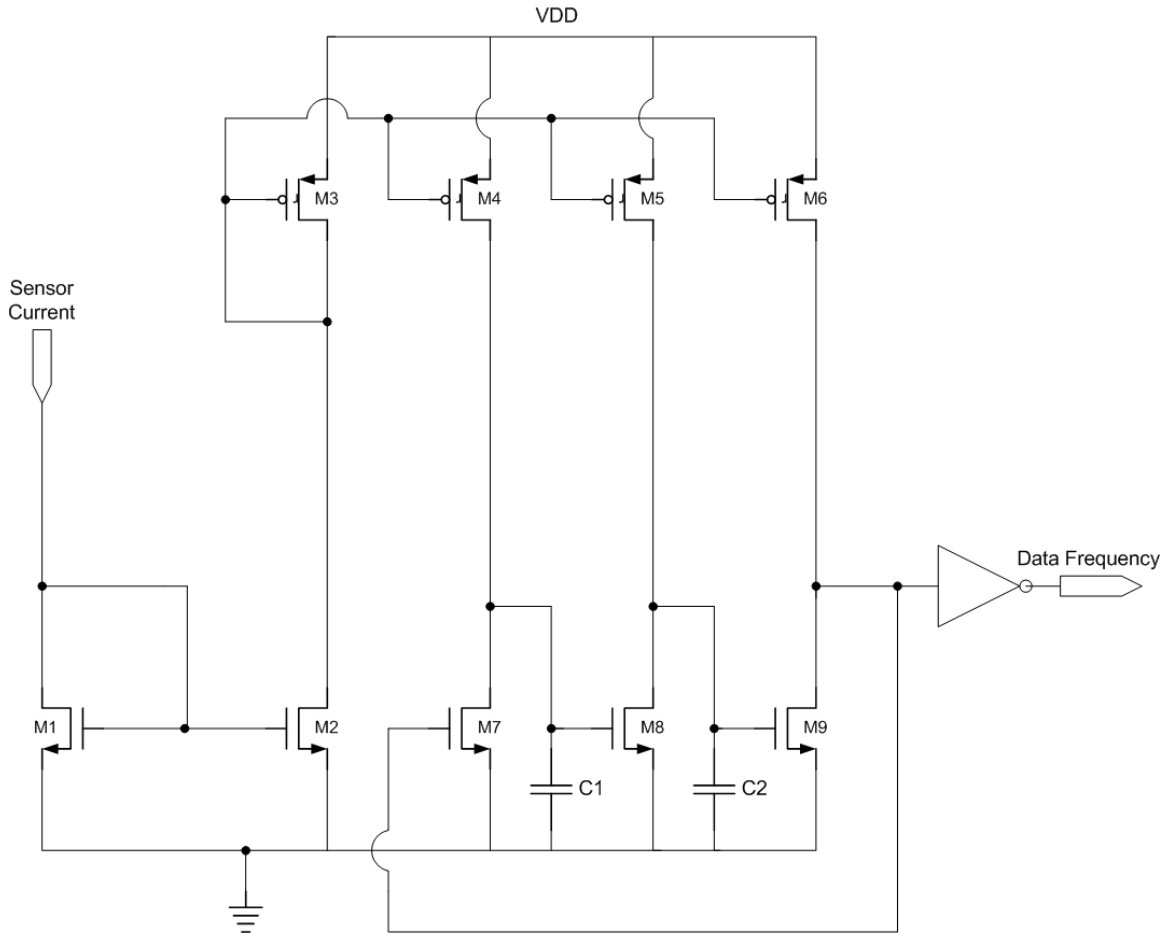


Fig. 3.1 Circuit diagram of data frequency generator

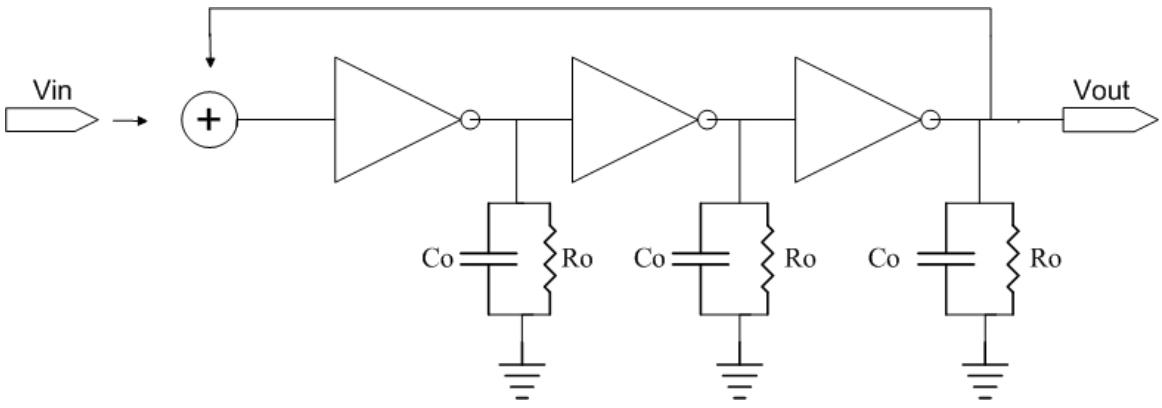


Fig. 3.2 Conventional circuit diagram of a ring oscillator

The factor of 2 in the above equation results due to both rising and falling edges of each delay stage contributing to f_{OSC}. From the above equation, it is obvious that there are two ways to change the frequency of oscillation: (1) by varying the number of delay stages, N and (2) by varying the delay per stage, T_d.

Let us assume that the gate to source parasitic capacitances, C_G of the NMOS and PMOS transistors are equal, then the frequency of oscillation will have following form,

$$f_{osc} = \frac{1}{2N\tau} \qquad (3.3)$$

where, τ is the delay of one inverter stage. The oscillation amplitude of each inverter stage is following:

$$V_{osc} = \int \frac{I_{ctrl}}{C_G} dt \qquad (3.4)$$

Combining above two equations, the delay of the inverter stage can be constructed as follows[12]:

$$\tau = \frac{V_{osc} C_G}{I_{ctrl}} \qquad (3.5)$$

,where V_{osc} is the oscillation amplitude, and I_{ctrl} is a controlling current from PMOS. This equation can be also applied to the CCO since current fed into NMOS is converted to voltage and transistors from M8 through M9 work as inverters. As a result, NMOS transistors as well as the last stage, which is an inverter, form a three stage ring oscillator as shown in Fig.3.2. By using a PMOS current source loads as a controlling source of a three-stage ring oscillator, CCO can achieve both a wide tuning range and a maximum speed, relatively independent of PMOS

device characteristics[10]. The PMOS loads will remain in saturation region because the voltage swings of the CCO are not rail-to-rail. Therefore, the gate-channel capacitance of the PMOS has negligible effect on the speed or the frequency. Since in this data frequency generator, relatively large capacitors have been in between M8 and M9, the parasitic capacitance on all PMOS as well as NMOS can be ignored. As a result, the frequency generated by this data frequency generator can be controlled by the size of C1 and C2 as well as currents flowing through the PMOS current mirrors. The carrier frequency generator was constructed in the same manner as the data frequency generator. Since the carrier frequency generator should generate the fixed frequency, a simple resistor R has been used in this design. Fig 3.3 shows the schematic of carrier frequency generator.

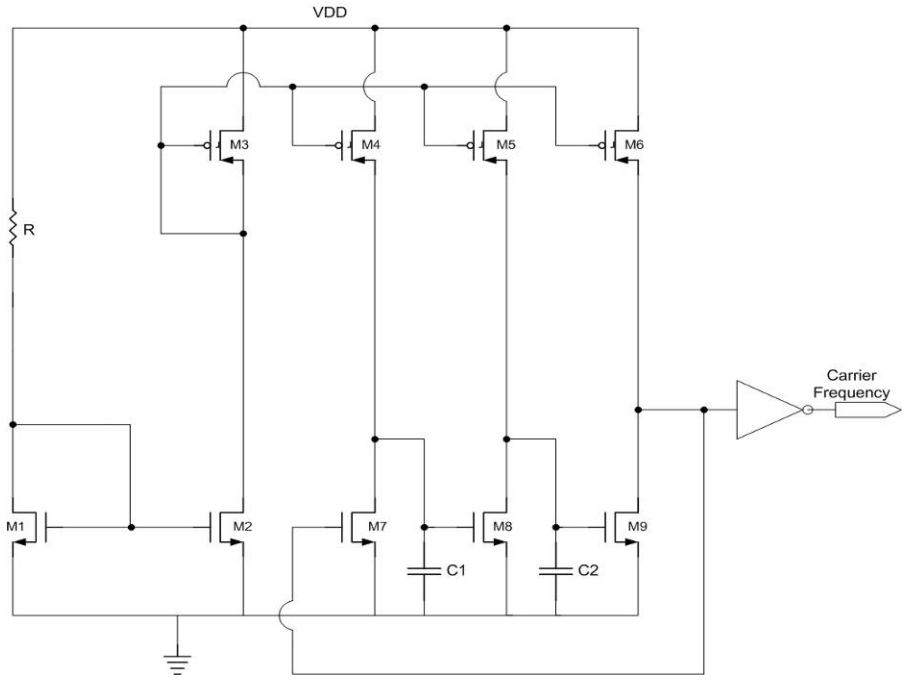


Fig. 3.3 Circuit diagram of carrier frequency generator

3.1.3 FSK Signal Generator

FSK modulation technique is one of the popular modulation techniques used in modern digital communication circuits. To produce the FSK signal, a designer should have three frequencies; that is a high carrier frequency, a low carrier frequency, and a data frequency. The FSK signal can be considered as the summation of two complementary ASK signals. For the comparison, Fig 3.4 shows an example of the ASK signal[7]. The output from the AND gate is modulated only when the data signal is high. Therefore, when the data signal is low, the modulated signal will be low as well. As a result, the output produces an ASK signal. However, unlike the ASK signal, the output of the FSK signal consists of two different signals, which are both high frequency and low frequency. To generate an FSK signal, scheme shown in Fig. 3.5 can be considered[13].

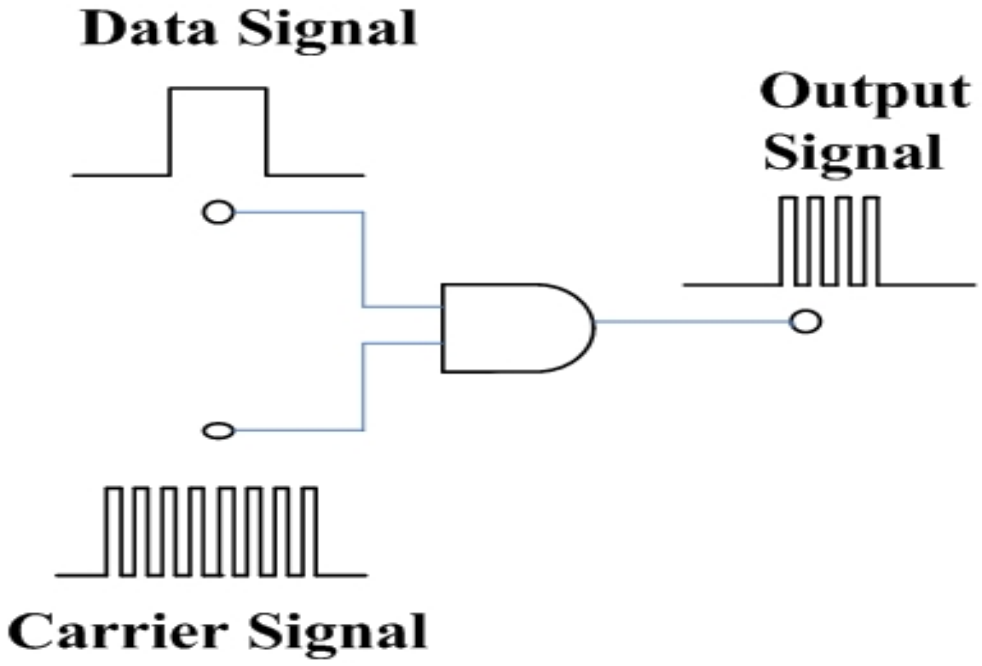


Fig. 3.4 An example of ASK signal

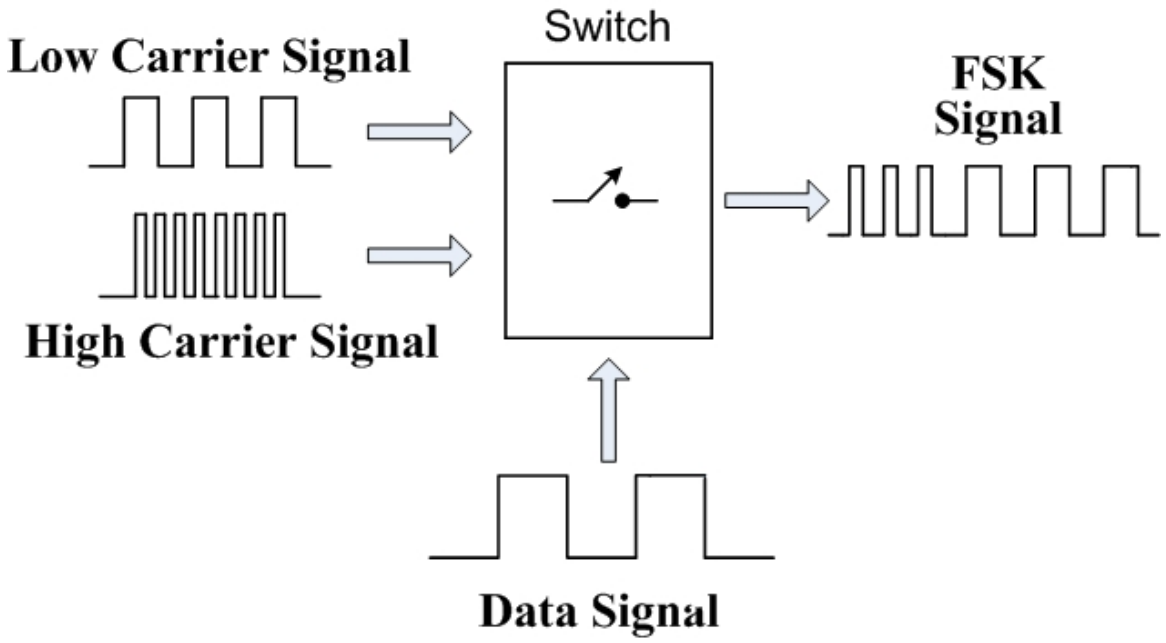


Fig. 3.5 An example of FSK signal

Low carrier frequency f_0 and high carrier frequency f_1 are fed into a switch, and a switch is controlled by the data frequency. A switch is continuously *on* and *off* as the data frequency goes high and low. When the data frequency goes high, for example, only the high carrier frequency passes through the switch, and when the data frequency goes low, low carrier frequency passes through the switch. The result of this modulation is similar to the output in Fig. 3.5, which is an FSK signal. For a current design, a 2:1 multiplexer has been used to replace a switch in Fig. 3.5.

When two different carrier frequencies are modulated together, a distortion or interference could occur. Thus when the frequency shifts from either high to low or from low to high, the

transition between each frequency could cause some distortion or interference problems. To prevent such an incident, only one carrier frequency generator has been used in this design.

In Fig. 3.3, this carrier frequency generator actually generates a high carrier frequency. To get a low frequency carrier, a divider is used. Fig. 3.6 shows the divider schematic[14]. The divided by 2 circuit uses two D flip-flops in a master-slave configuration with negative feedback. Generally, in high speed master-slave dividers, designing the slave as the "dual" of master is a common way. The reason is that both D latches are driven by one clock. The problem of this duality is that this technique requires one of the latches to incorporate the PMOS devices in a signal path. However, this will cause lowering the speed. To overcome this problem, two identical D flip-flops that are sharing one clock are used. Usually in high frequency operation, clock skew could occur in this topology. To eliminate the clock skew problem if there is any, a designer can put a complementary pass gate to equally distribute the clock signal into the CK[14]. Fig. 3.6 shows the divided output signal of Fig 3.5 topology.

As a final stage of FSK modulator, Fig 3.8 shows how the FSK signal can be produced. High carrier frequency that is generated by the carrier frequency generator directly feeds into the multiplexer, and the very same frequency is fed into the divider circuit to produce a low carrier frequency. Data frequency has been used to control the select bit of 2:1 MUX. The final result is the FSK signal, which is of interest in this design.

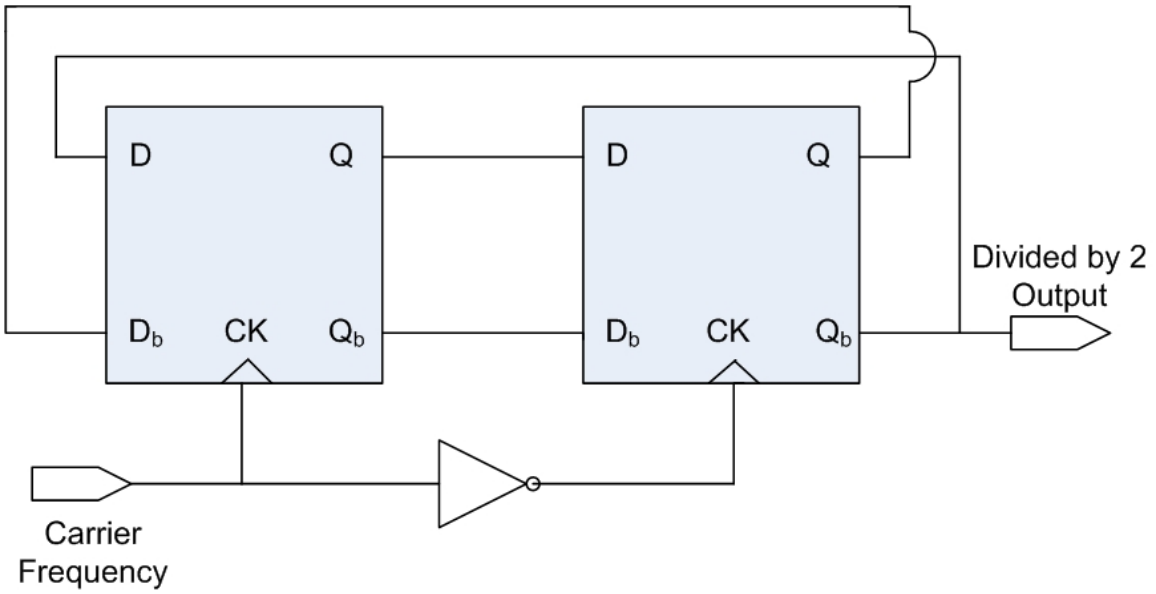


Fig. 3.6 Conventional circuit diagram of divided by 2

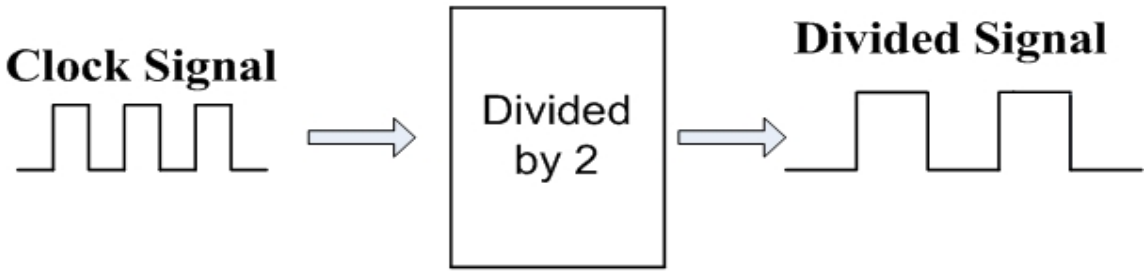


Fig. 3.7 Divided by 2 output signal

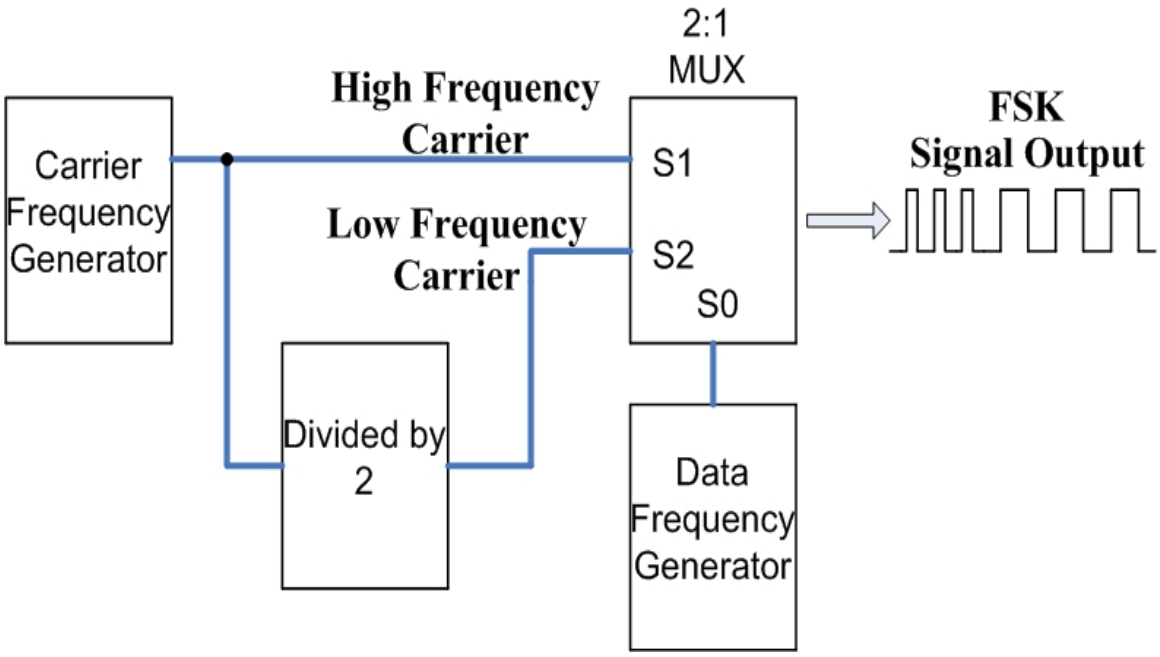


Fig.3.8 Block diagram of a FSK signal modulator

3.2 The Bandgap Circuit Design

3.2.1 A Bandgap Reference Circuit

In analog design, one of the essential building blocks is a voltage reference circuit, which should be able to provide a stable voltage over the temperature changes, ideally independent of a supply voltage, and the fabrication process. For example, in ADC, a stable biasing reference voltage is important because a reference voltage is required to quantify an input. Also, in DAC, a reference voltage is required to define the output full-scale range. Among various a well-defined reference voltage generator techniques, a bandgap reference is one of the most popular topologies for Bipolar, CMOS or BICMOS processes. The principle of operation of the bandgap reference circuit depends on two diode-connected bipolar junction transistors (BJT), which are operating at

different emitter current levels. By canceling the negative temperature dependence of the *pn* junctions in one group of transistors with the positive temperature dependence from a proportional-to-absolute-temperature (PTAT) circuit which contains the other group of transistors, a fixed stable DC voltage is generated without any variances with temperature changes. Usually, this reference voltage is 1.26V, and this voltage is approximately the same as the bandgap of silicon.

3.2.2 Bandgap Circuit Design

There are many kinds of circuit topologies out there to produce a stable and a temperature independent reference voltage, but a bandgap reference voltage circuit is the most widely used topology. Mainly, a bandgap reference voltage circuit has a supply-independent biasing circuit, a diode-connected BJT transistor generating a voltage with a negative temperature coefficient, a PTAT current, and for a better performance, a feedback mechanism. In this design of a bandgap reference circuit, current mirrors with current feedback system have been used to reduce supply dependence[15, 16]. For a feedback system, a simple two-stage single-ended PMOS input differential amplifier has been used. More about a differential amplifier will be discussed in section 3.3.

A reference voltage is generated by putting two voltages with opposite sign of temperature coefficients along with suitable multiplication constant. The two voltages that have an opposite temperature coefficient are V_{BE} and V_T. Typically in BJT, V_{BE} has a temperature coefficient of -2.2 mV/^{o}C and V_T has a temperature coefficient of +0.085 mV/^{o}C.

Fig. 3.10 explained the principle of how the positive temperature coefficient (TC), and negative TC can be added together, so that two opposite sign of TC could be cancelled out to achieve the dependence of temperature in circuit level, where V_T is the thermal voltage, k is Boltzmann's constant, q is the electron charge, m is the ratio of the current densities of two BJTs, and T is the absolute temperature[15].

Back to the Fig. 3.9, a current I_1 is passing through Q_1, which comes from a supply independent current source[16-18]. Also, the same current is flowing in the branch of Q_2 of which m BJTs are connected in parallel. The voltage difference between V_{BE1} and V_{BE2} can be expressed as follows.

$$V_{BE1} - V_{BE2} = \Delta V_{BE} = V_T \ln\left(\frac{I_1}{I_S}\right) - V_T \ln\left(\frac{I_2}{mI_S}\right) = V_T \ln(m) \qquad (3.6)$$

Fig. 3.11 shows the complete diagram of the bandgap reference circuit used in this design. The output voltage at R2 is given by[18],

$$V_{ref} = V_{BE3} + \frac{V_T \ln(m)}{R_1} R_2 = V_{BE3} + IR_2 \qquad (3.7)$$

,where $I_{Diode} = I_S e^{\left(\frac{V_{BE}}{V_T}\right)}$, $I = I_1 = I_{2.}$, and $I_1 = I_2 = \frac{V_T \ln(m)}{R_1}$

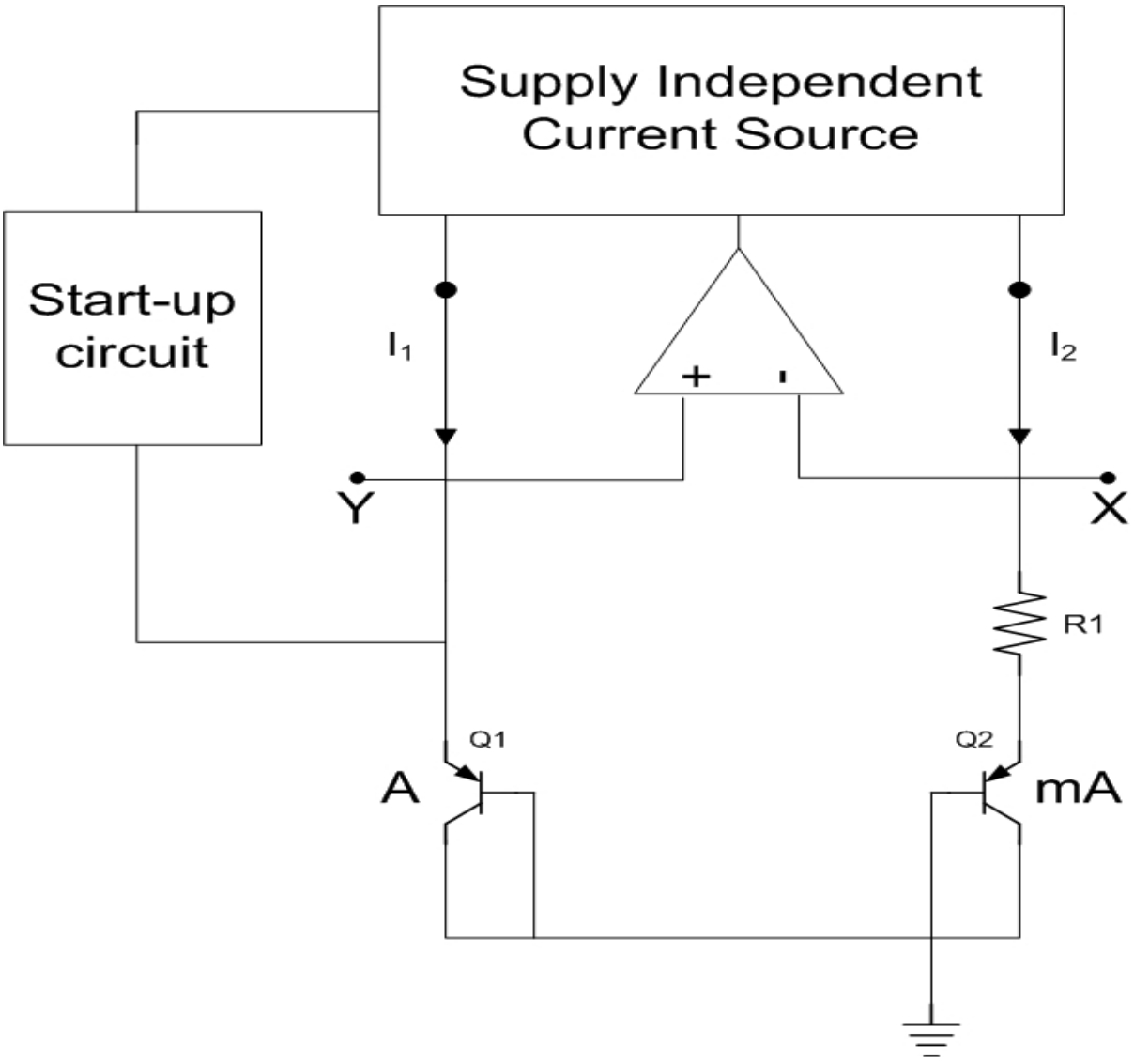


Fig.3.9 Block diagram of a bandgap reference voltage circuit

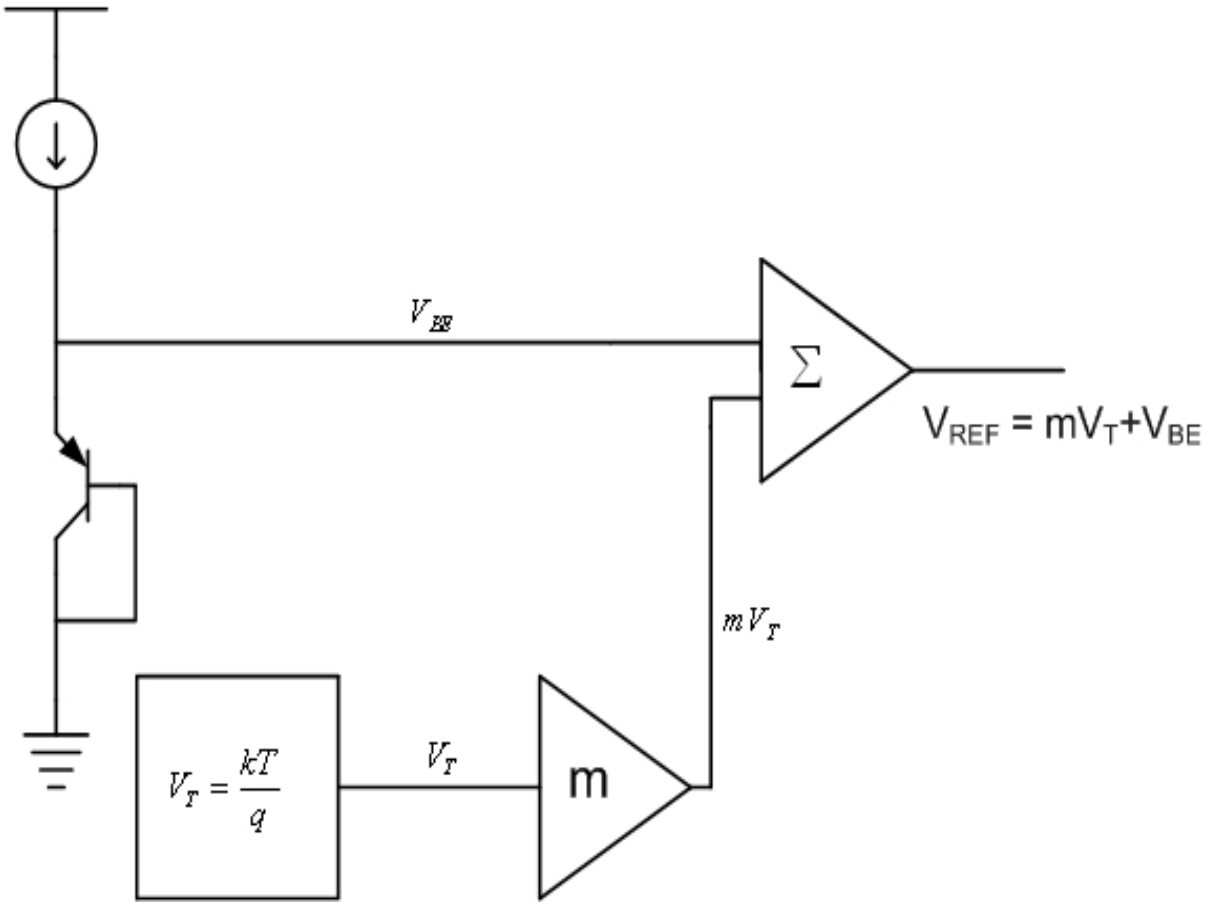


Fig. 3.10 Principle of operation of the bandgap reference voltage circuit

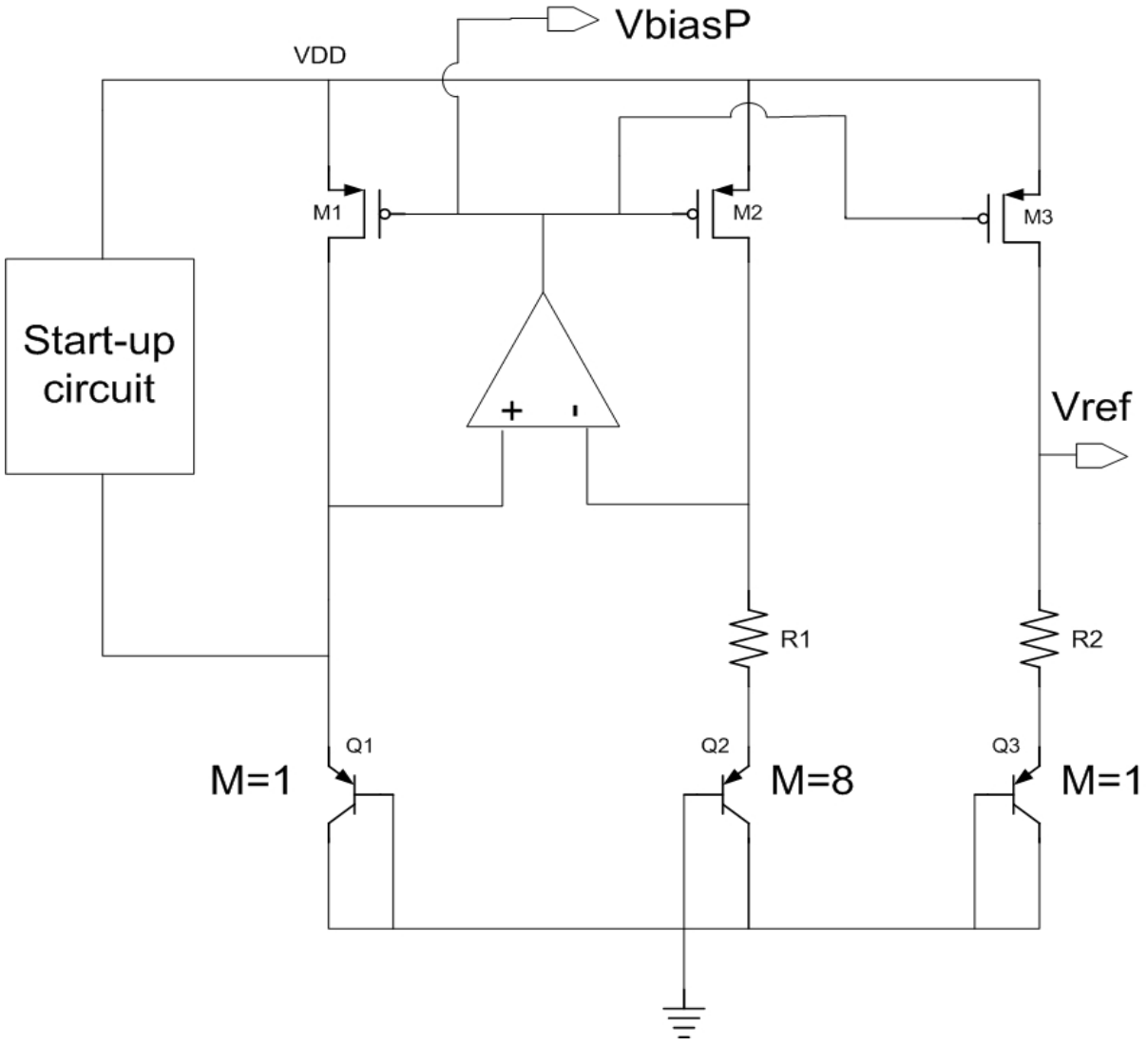


Fig. 3.11 Circuit diagram of a bandgap reference voltage circuit

3.2.3 Start-Up Circuit Design

This bandgap reference circuit should have some sort of start-up circuit. Fig. 3.12 shows the start-up circuit. Initially, all transistors in a bandgap reference are in "off" state, and C_1 in Fig. 3.12 has no charge on it. As a result, PMOS of M2 turns on and M1 turns on as well resulting is a current in Q1 as well as in M2 and M3. Since a current is flowing in M1, C_1 starts charging. When the capacitor is fully charged, it will force M2 to "off" state and M1 thereafter. Therefore, the circuit stops its function as a start-up circuit.

3.3 Operational Amplifier Circuit Design

3.3.1 Operational Amplifier

In analog design, an operational amplifier (Op-Amp) is perhaps the most important, and most widely used fundamental circuit, which is usually, a part of other analog and mixed signal circuits. Compared to BJT oriented Op-Amps, CMOS Op-Amps have typically a lower transconductance for a given current level, lower gain, slower speed, higher input-referred offset, and input-referred noise voltage[18]. However, current trends of technology are more and more towards combining the digital and the analog circuits integrated together in a CMOS process. For example, analog signals are quite often needed to be interfaced to digital signals or vice versa in many complex systems such as an analog-to-digital converter, a digital-to-analog converter, and so forth. CMOS technology is becoming more dominant than BJT technology because it offers several advantages such as smaller size, less power consumption, and flexibility of combining with digital circuits.

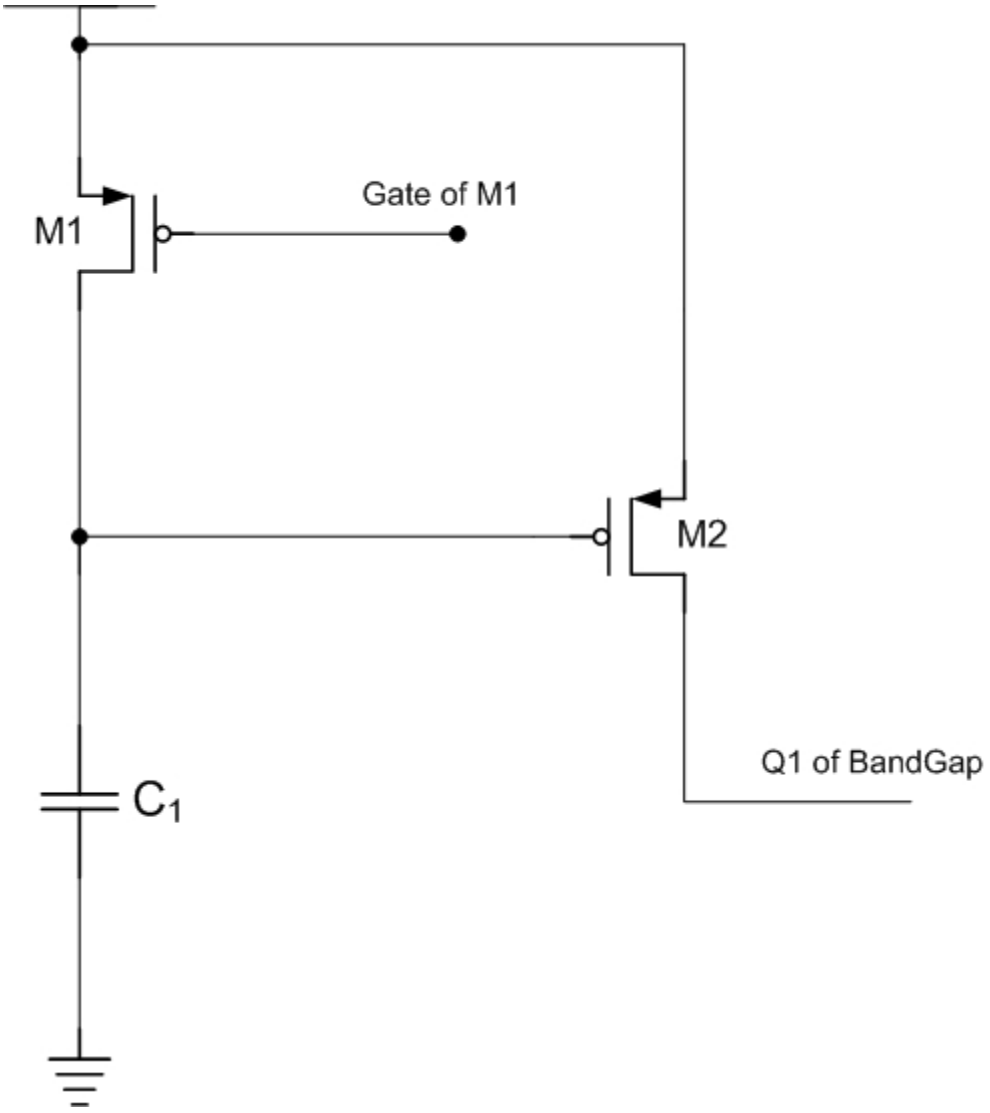


Fig. 3.12 Circuit diagram of a start-up

3.3.2 Two-Stage Operational Amplifier

The most widely used topology for the operational amplifier is a two-stage amplifier since it can achieve a good common mode range, output swing, voltage gain and so forth. Fig 3.13 shows the four functional block diagram used in this design.

The fist block is for an input differential gain amplifier. The second block converts the signal from the first block to a single-ended signal since the following block has an input which is referenced to ground.

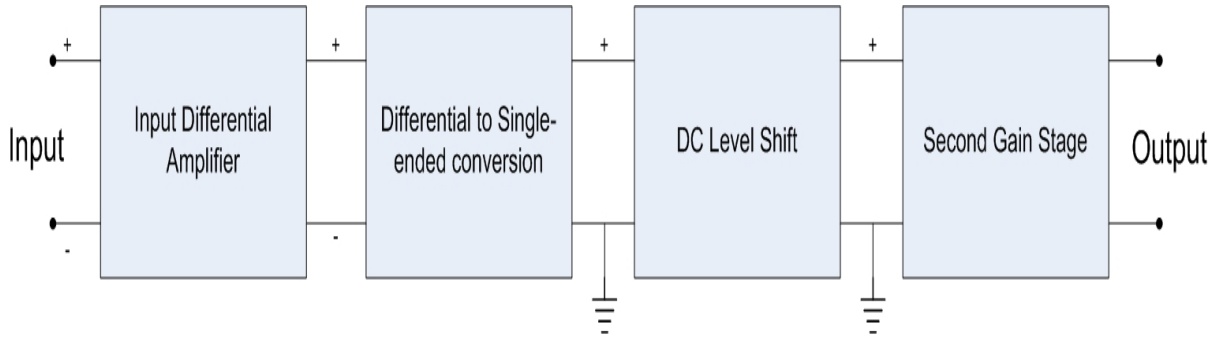


Fig. 3.13 Functional block diagram of an Op-Amp

The third block is for DC level-shift, which is for properly biasing the second gain stage. At the last block, a second gain stage is used to provide an additional gain. Fig. 3.14 shows the actual schematic of the basic two-stage amplifier of this design[18, 19]. The first stage of operational amplifier is the most important part of designing an Op-Amp. This input stage has a capability of amplifying the difference between the two inputs and rejecting the common signals in both inputs. For example, the input pairs can reject the common-mode signals such as the common noise signal, the variation in the power supply voltage as a function of time and so forth. The PMOS transistors M1 and M2 are used as input devices and M3 and M4 are used as load. A

PMOS input pairs has been chosen because a PMOS input pair differential amplifier can detect a signal as low as the ground signal so that this Op-Amp can be used in a bandgap reference circuit. In addition, the PMOS transistors usually have lower noise than NMOS of equal size of transistor and similar bias conditions. M3 and M4 are active loads for the differential pairs and they will provide conversion of the differential signal to a single ended output signal of the first stage. M8 provides the biasing current for M5.

As shown in Fig. 3.14, the current I_{bias} which is flowing through M8 as well as the transistor M5 (let us call it as I_{D5}). Assuming that M1 through M4 are perfectly matched to one another, then the current flowing M1 through M4 is just half of the current flowing in M5, which is $\frac{I_{D5}}{2}$.

The general equation for the drain current is given below as,

$$I_D = \left(\frac{1}{2}\right)\mu C_{ox}\left(\frac{W}{L}\right)\left(V_{GS} - V_{Th}\right)^2 \qquad (3.9)$$

where, the channel length modulation is ignored, μ_n and μ_p are the mobility of n-type and p-type materials, V_{Th} is the threshold voltage of either p- or n-type material, C_{ox} is the oxide capacitance per unit area.

M3 is a diode connected MOSFET, and its V_{gs3} is same as V_{ds3}. Since M3 and M4 are forming a simple current mirror, V_{gs3} should be also mirrored to V_{gs4}. As a result, the current that is flowing through M3 should be mirrored to M4 as well if the two transistors have same W/L ratio

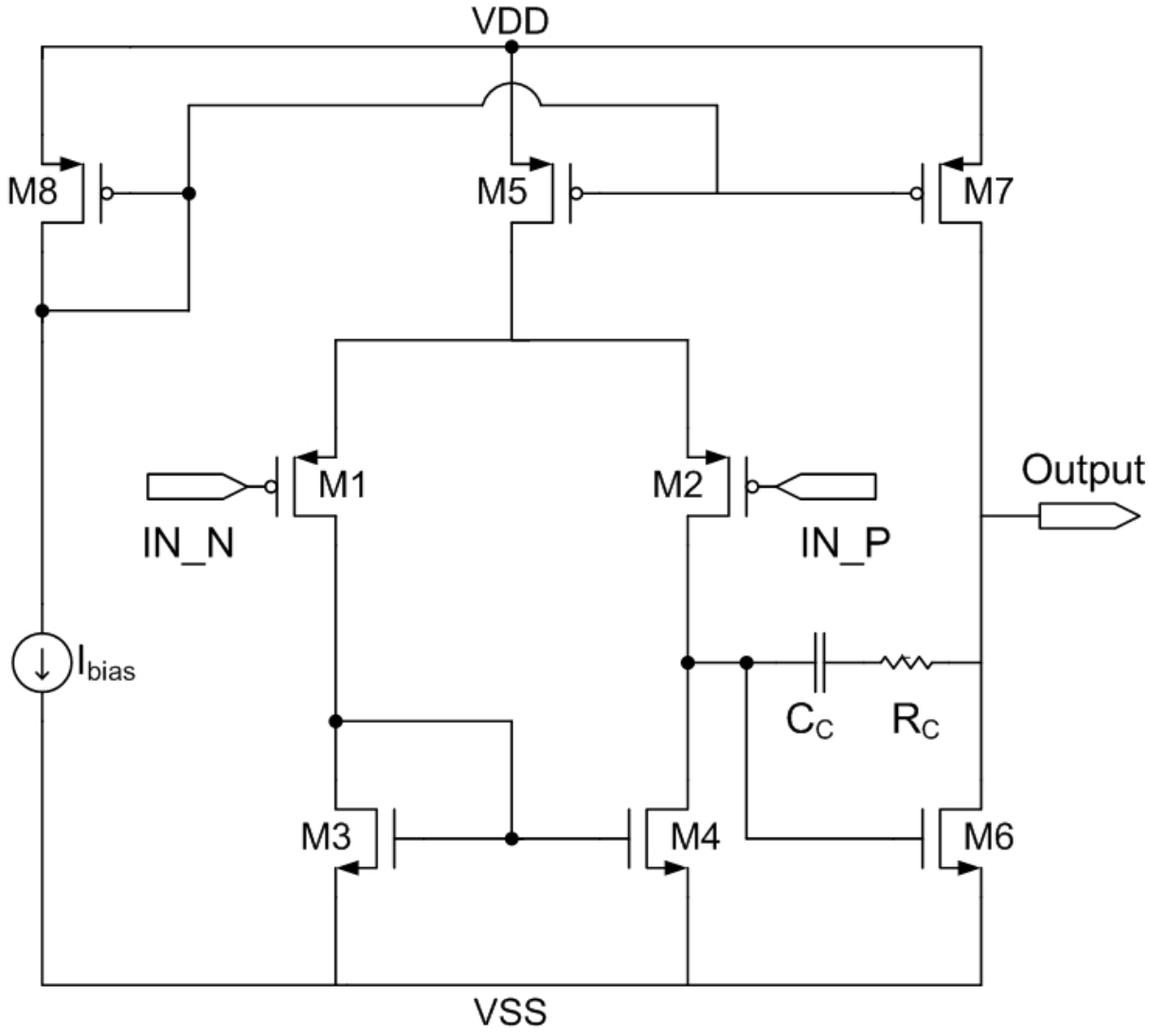


Fig. 3.14 Circuit diagram of a two-stage Op-Amp

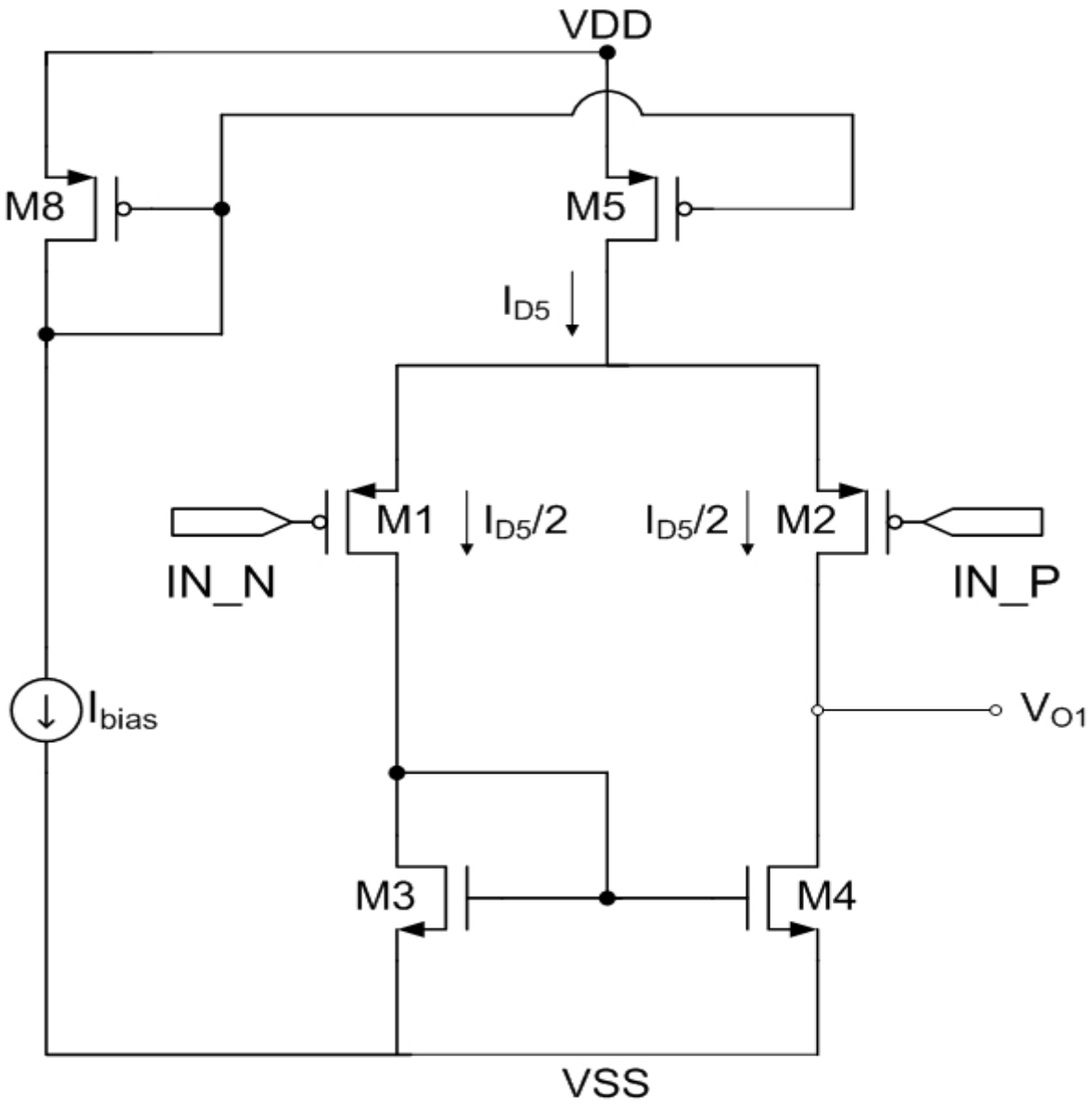


Fig. 3.15 Circuit diagram of a differential stage of an Op-Amp

Since $V_{GS3} = V_{GS4} = V_{DS4}$, the drain-source voltage of M4 can be expressed as[18],

$$V_{DS4} = V_{GS3} = V_{Th} + \sqrt{\frac{I_{D5}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_3}} \tag{3.10}$$

When the input voltage of IN_N and IN_P are zero, V_{O1} can be expressed as[18],

$$V_{O1} = V_{SS} + V_{gs3} = V_{SS} + V_{ov4} + V_{DS4} \approx V_{Th} + \sqrt{\frac{I_{D5}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_3}} \tag{3.11}$$

Gain of the first differential input stage is given by[18],

$$A_{v1} = g_{m1}\left(r_{o2} \| r_{o4}\right) \tag{3.12}$$

and the second stage gain is given by[18],

$$A_{v2} = -g_{m2} R_o \tag{3.13}$$

where, R_o is equal to $r_{o6} \| r_{o7}$

Therefore, the total gain of this two-stage amplifier can be expressed as,

$$A_v = A_{v1} A_{v2} = -g_{m1}\left(r_{o2} \| r_{o4}\right) g_{m6}\left(r_{o6} \| r_{o7}\right) \tag{3.14}$$

This total gain is related to $\left(g_m r_o\right)^2$, and $g_m r_o$ can be expressed as $\frac{2V_A}{V_{ov}}$ [18].

Therefore, the overall gain of this amplifier is strongly tide to both the Early Voltage V_A, which is proportional to effective channel length, and the overdrive voltage, which is determined by the bias conditions.

A feedback capacitor C_C, which is called as "Miller Compensation Capacitor" is added between the drain of M4 and M6[19]. The function of this feedback capacitor is to ensure that Op-Amp has sufficient phase margin, which is a factor of whether the circuit operates in a stable conditions or not. Since the devices in Op-Amp always have some parasitic capacitances, the voltage gain decreases as the frequency increases. Therefore, to rectify this drawback, a compensation capacitor should be added to ensure that the circuit does not oscillate when it is connected in a feedback loop. However, adding a compensation capacitor also creates a zero pole, which can cause the oscillation in an Op-Amp. To eliminate this problem, R_C should be added to ensure the performance of the circuit in a feedback loop.

The small signal equivalent circuit of the two-stage amplifier can be modeled as shown in Fig 3.16[19]. The non-dominant poles due to the capacitances at the source of M1 and M2, the capacitance at the gate of M3 and any other non-dominant poles are neglected since they have negligible effect on the circuit performance. The circuit has two poles and one zero, and those three poles can be approximately expressed as follows[18, 19],

$$P_1 = \frac{-1}{(1 + g_m R_2) C_C R_1} \tag{3.15}$$

$$P_2 = \frac{-g_{m2} C_C}{C_1 C_2 + C_2 C_C + C_C C_1} \tag{3.16}$$

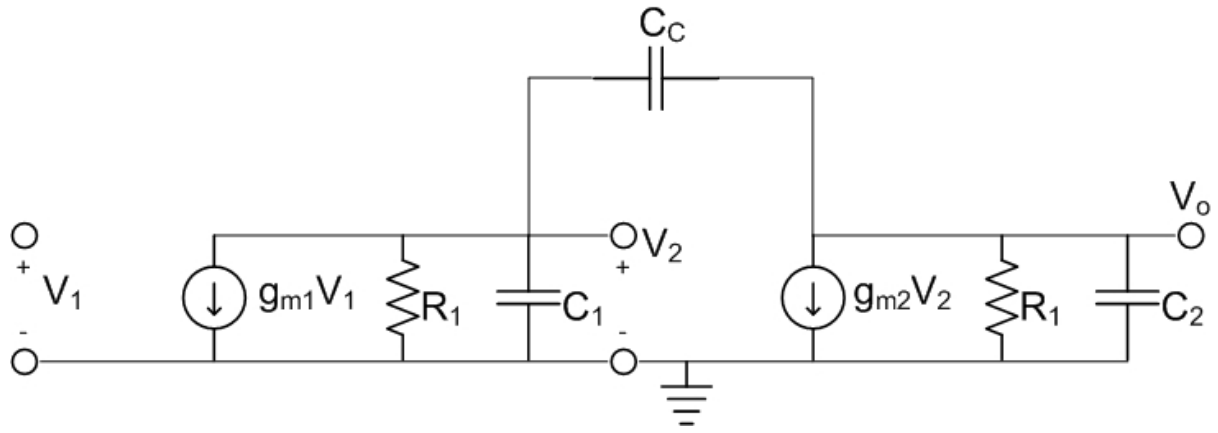


Fig. 3.16 Small signal equivalent circuit for the two-stage amplifier

$$Z = \frac{+g_{m2}}{C_C} \tag{3.17}$$

The pole due to the capacitive load of the first stage P_1 has been pushed to low frequency by the Miller effect in the second stage, and the pole due to the capacitance at the output of the second stage, P_2, has been pushed to high frequency. This technique is called as a pole splitting since P_1 and P_2 are separated from each other. Usually, phase margin of 60^o gives enough space for the circuit so that the circuit will not oscillate. To get a 60^o of a phase margin, choosing the value of C_C as follows[15],

$$C_C \rangle 0.22 C_L \tag{3.18}$$

However, this value will not guarantee that the phase margin will have more than 60^o, so careful simulation should be performed. Fig. 3.17, 3.18 shows the diagram before and after a compensation network is added[15].

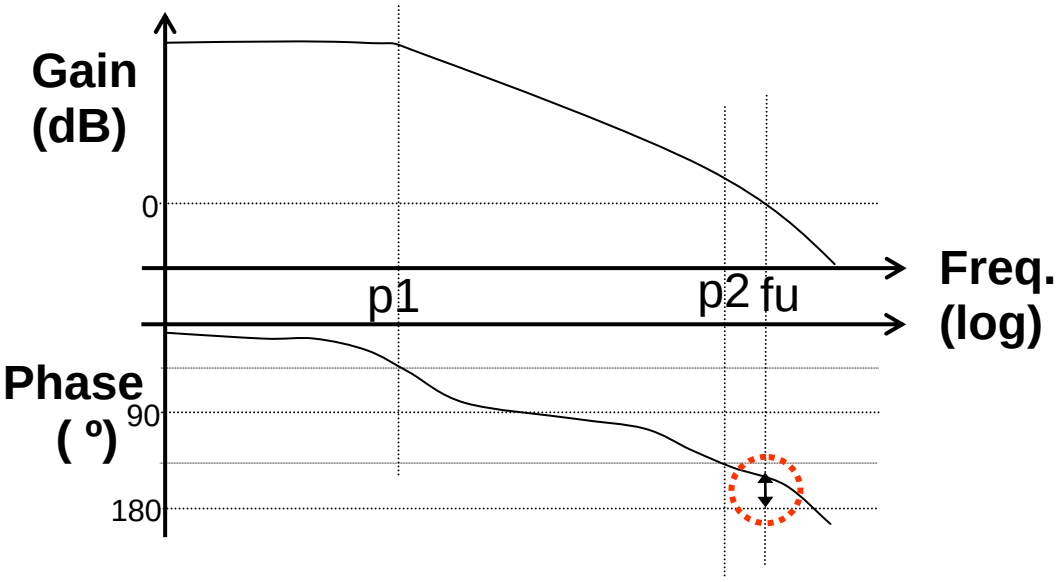
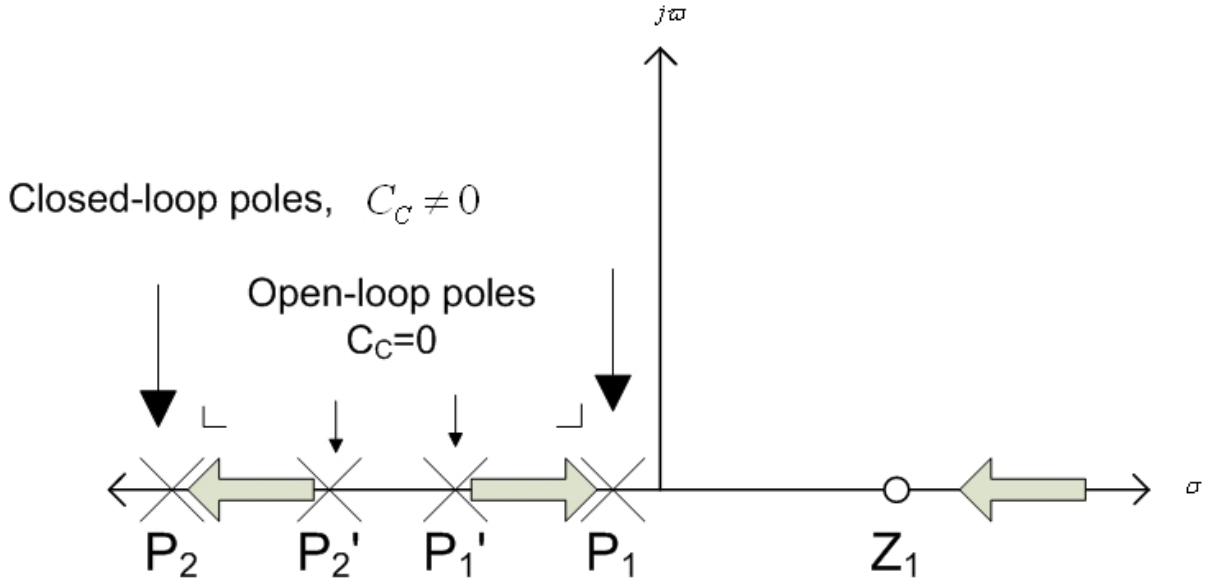


Fig. 3.17 Bode diagram of the two-stage amplifier before compensation network added



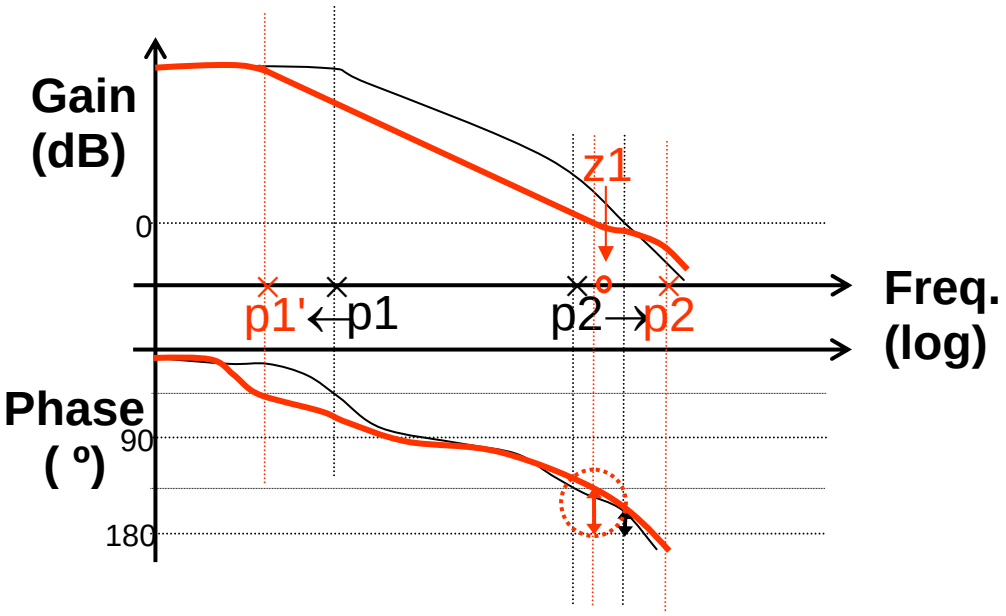


Fig. 3.18 Bode diagram of the two-stage amplifier added after compensation network added

The slew rate (SR) is defined as the maximum change rate of the output of the Op-Amp. The SR in general, describes the degradation effect on the high frequency response of the active amplifier near or at the rated maximum output voltage swing. This effect is generally due to the compensating capacitor and not to the transistors inside of the Op-Amp. In short, the SR effect is due to the maximum supplied current available for charging up the compensation capacitor. The slew rate in two-stage amplifier can be expressed as[20],

$$SR = \frac{dV_{out}}{dt}\Big|_{MAX} = \frac{I_{C_C}\big|_{MAX}}{C_C} = \frac{I_{TAIL}}{C_C}\frac{I_{D5}}{C_C} \tag{3.19}$$

$$\therefore \mathrm{SR} = \frac{I_5}{C_C} \tag{3.20}$$

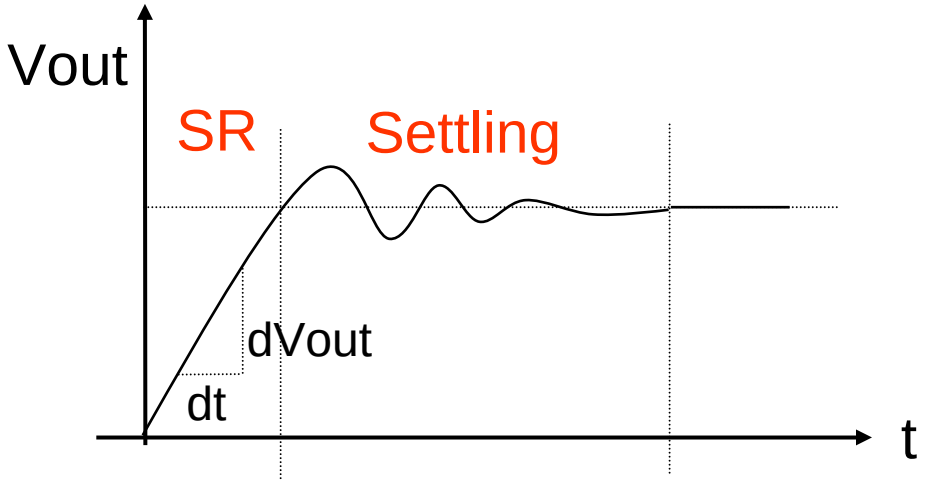


Fig. 3.19 Output voltage waveform showing the slew rate

Fig. 3.18 shows graphical solution of the slew rate.

There are two kinds of input offset voltages in an operational amplifier. One is the systematic offset and the other is the random offset. The random offset occurs because of the mismatch of the devices, and threshold voltage mismatch in input transistors. To reduce the random offset voltage, in Fig. 3.13, longer channel lengths of M3 and M4 are selected. By looking below equation one can see that by reducing the W/L ratio of the load devices, M3's and M4's tranconductances can be smaller than those of M1's and M2's. Also, careful layout of input pairs as well as the loads is helpful to reduce the input offset voltage. The random offset voltage is given by[19]

$$V_{OS} = \Delta V_{t(1-2)} + \Delta V_{t(3-4)}\left(\frac{g_{m3}}{g_{m1}}\right) + \frac{V_{ov(1-2)}}{2}\left[\frac{\Delta\left(\frac{W}{L}\right)_{(3-4)}}{\left(\frac{W}{L}\right)_{(3-4)}} - \frac{\Delta\left(\frac{W}{L}\right)_{(1-2)}}{\left(\frac{W}{L}\right)_{(1-2)}}\right] \tag{3.21}$$

Even if the matching of the devices is perfect, still, the systematic offset exists. To explain the systematic offset, let us assume that the two input pairs are connected to the ground and the matching of the devices is perfect. Then, V_{DS4} should be equal to V_{GS3}, and V_{DS1} should be equal to V_{DS2} as well. Under these conditions, the relationship of $I_{D1} = I_{D2} = I_{D5}/2$ can be established[18, 19]. The V_{GS} of M6 is required to set the output voltage of the amplifier at the midway between V_{DD} and $V_{SS,}$ and V_{GS6} may differ from the DC output voltage in first stage. To set the value of the output voltage of the second stage to the middle of the power supply voltage, V_{GS6} should be carefully chosen so that the current flowing in M6 and M7 are the same so that M6 and M7 can fall into the saturation region. Since M3 is a diode-connected device and M3 and M4 form a current mirror, V_{GS3} and V_{GS4} are the same, and V_{GS4} is the same as V_{DS4} as well. As a result, the transistor M4 can be considered to be virtually a diode-connected transistor. At the same time, since the gate of M6 is connected to the drain of M4, V_{DS4} should be also the same as V_{GS6}. These conditions will cause the overdrive voltages of M3, M4, and M6 to be the same. Moreover, we assumed the devices are matching perfectly, threshold voltages of M3, M4, and M6 should be same.

Therefore[18, 19],

$$V_{ov3} = V_{ov4} = V_{ov6} \tag{3.22}$$

Equation (3.22) leads to the following equations.

$$\frac{I_{D3}}{\left(\frac{W}{L}\right)_3} = \frac{I_{D4}}{\left(\frac{W}{L}\right)_4} = \frac{I_{D6}}{\left(\frac{W}{L}\right)_6} \tag{3.23}$$

Since $I_{D3} = I_{D4} = I_{D5}/2$, and $I_{D6} = I_{D7}$,

$$\frac{I_{D5}}{2\left(\frac{W}{L}\right)_3} = \frac{I_{D5}}{2\left(\frac{W}{L}\right)_4} = \frac{I_{D7}}{\left(\frac{W}{L}\right)_7} \tag{3.24}$$

Since the gate source voltages of M5 and M7 are same,

$$\frac{I_{D5}}{I_{D7}} = \frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_7} \tag{3.25}$$

Combining these equations, we can get,

$$\frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_6} = \frac{\left(\frac{W}{L}\right)_4}{\left(\frac{W}{L}\right)_6} = \frac{\left(\frac{W}{L}\right)_5}{2\left(\frac{W}{L}\right)_7} \tag{3.26}$$

If this relationship is satisfied, the current densities of M3, M4, and M6 should be equal, and therefore, there should be no systematic offset voltage at the input.

3.4 Operational Amplifier with Buffer Stage Circuit Design

3.4.1 Operational Amplifier with Buffer Stage

In an ideal operational amplifier, R_{IN} is infinite, and R_{OUT} is zero. As a result, the Op-Amp ideally, can drive any load. However, reality is not the same as an ideal case. The two-stage operational amplifier given in previous section is actually called as an Operational Transconductance Amplifier (OTA). OTA can drive only small resistive loads or mainly capacitive loads. As a result, the OTA circuit analyzed in previous section is built to use in the bandgap reference circuit and the voltage regulator, which will be discussed in the next section. Basically, the design of the output buffer of a two-stage Op-Amp is the same as discussed in the

previous section except for the design of the buffer stage. Therefore, only the buffer stage will be discussed in this section.

In Fig. 3.20, the building blocks of the two-stage Op-Amp with buffer are as follows:

- A1 : Differential to Single Ended Conversion
- A2 : Gain Stage & Compensation
- X1 : Buffer for resistive load or large capacitive load

Fig 3.20 is a simplified version of Fig 3.21. Fig. 3.20 shows how the output buffer stage is added to conventional two-stage Op-Amp[19]. From Fig. 3.21, it is easy to see that two NMOS transistors, M9 and M10, have been added to a conventional two-stage Op-Amp as a buffer stage. Transistors M9 and M10 actually form a source follower configuration. Fig. 3.22 shows a redrawn picture of M9 and M10 as source follower configuration. Since the source follower has an output impedance looking into source of M9 given by[16],

$$R_{out} = \frac{1}{g_{m9} + g_{mb9}} \tag{3.27}$$

which, is smaller than R_{out} of Op-Amp without the buffer stage. As a result, this Op-Amp can drive higher resistive loads than conventional two-stage Op-Amp without a buffer stage.

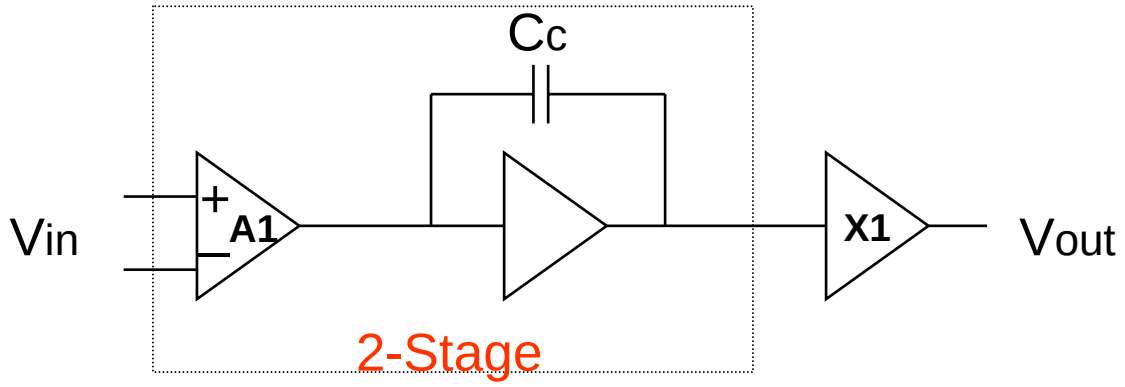


Fig. 3.20 Block diagram of the two-stage Op-Amp with buffer

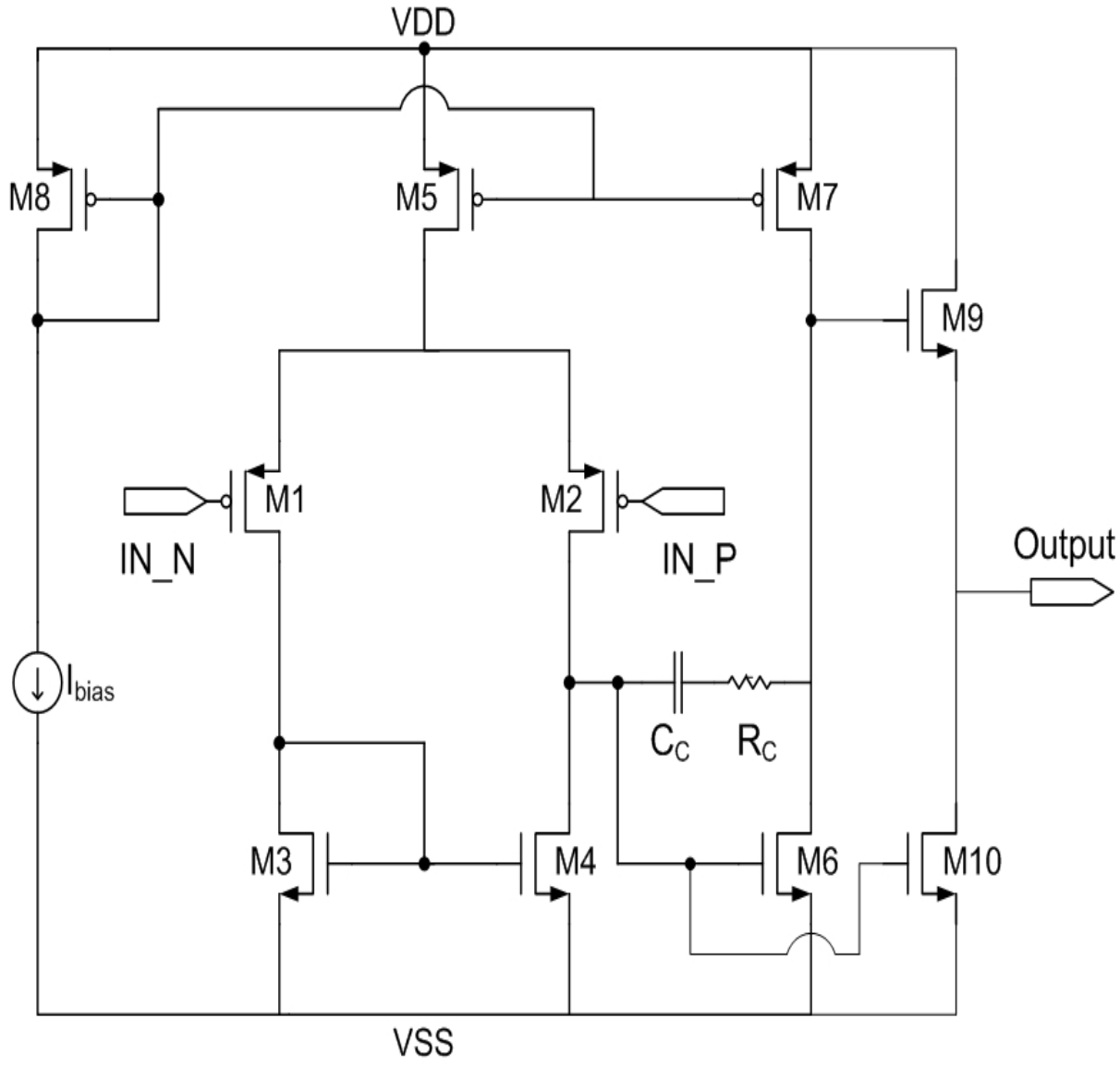


Fig. 3.21 Circuit diagram of the two-stage Op-Amp with buffer

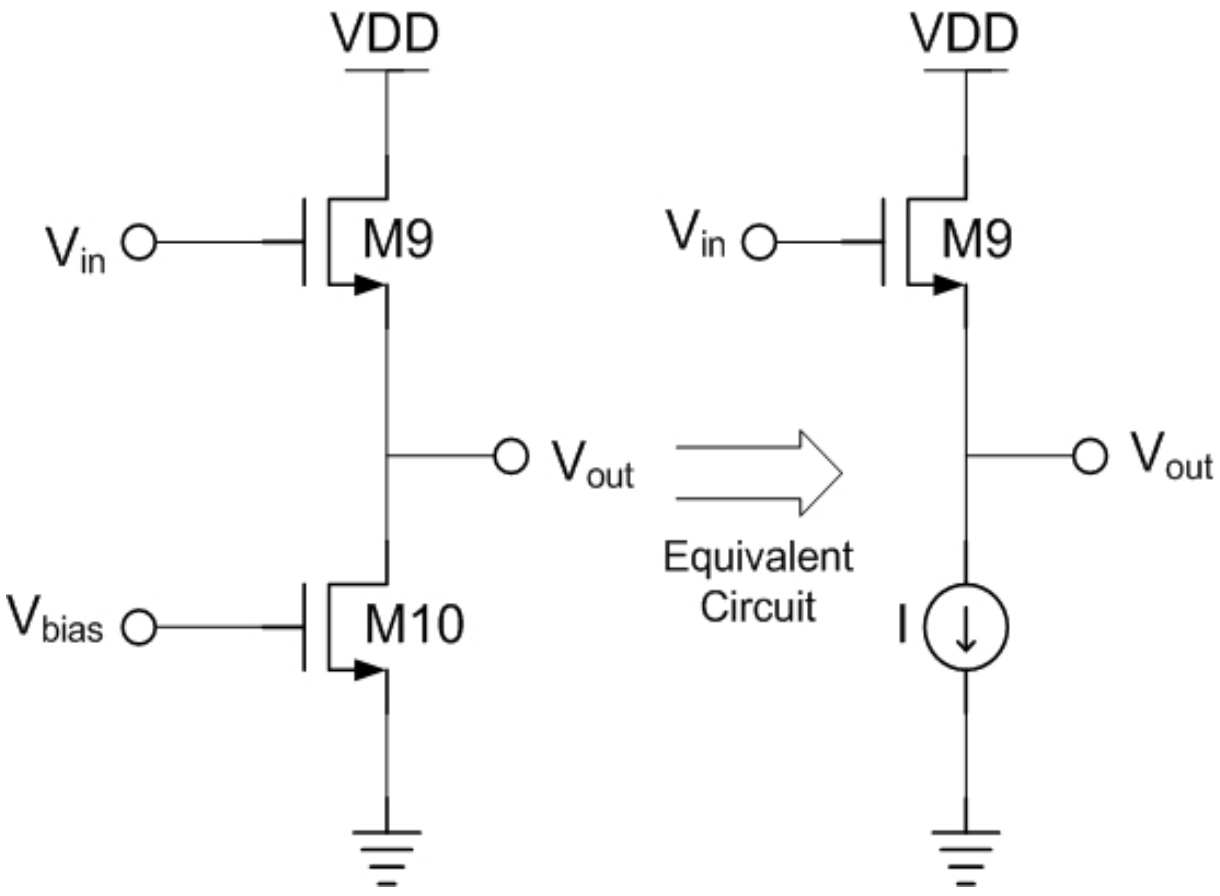


Fig. 3.22 Schematic of source follower buffer stage

3.5 Voltage Regulator Design

3.5.1 Voltage Regulator

Any electrical systems require having some sort of power supply. As the resolution of the fabrication processes are becoming finer and finer, smaller and portable electronics are being produced more and more. At the same time, the power supply voltage is getting lower and lower. Therefore, precisely controlled power supplies are currently being demanded and required by many applications. A voltage regulator is the one that can provide such a controlled level of supply voltage to the system. The function of a voltage regulator is to reduce the voltage variation of the power supply, such as a battery, towards acceptable and stable levels[21]. Without these voltage regulators, a system will not work properly or even fail to work. Therefore, having a good voltage regulator is one of the most important key components of a stable and reliable system in all analog/mixed signal designs as well as in digital designs. In this design, a low voltage drop-out voltage regulator (LDO) is presented. Fig 3.23 shows the basic diagram of linear regulator[22-24].

A linear voltage regulator uses a voltage-controlled current source to have a fixed output voltage across a load resistor. The control circuit (OTA) is monitoring the output voltage in a load and accordingly, adjusting the current level, which is flowing in a load resistor to have a constant and stable output voltage[23]. The output voltage is controlled by the feedback loop, and this feedback requires some kind of compensation to assure a stable operation. Some voltage regulators like low dropout voltage regulator are required to have an external capacitance connected to the output for a stable operation

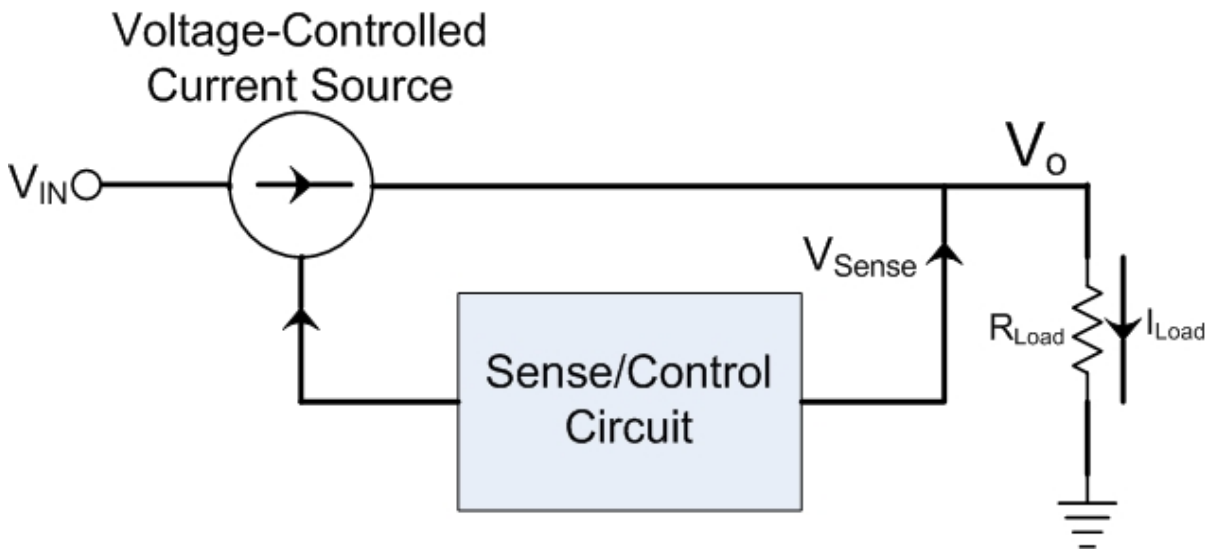


Fig. 3.23 Conventional diagram of a linear voltage regulator

3.5.2 Low Drop-Out (LDO) Voltage Regulator

Fig. 3.24 shows the actual circuit diagram that has been used in this design[7]. A low drop-out voltage regulator (LDO) provides a very small input-output differential voltage in DC. In the LDO, a positive input of the differential amplifier monitors the value that is determined by R_1 and R_2. A negative input of the differential amplifier is from a stable voltage, which is derived from a bandgap reference circuit. The OTA constantly monitors and compares the value of the voltage between R1 and R2 with the reference voltage so, if the output voltage rises too high compared to the reference voltage, the drive to PMOS changes so as to maintain a constant output voltage.

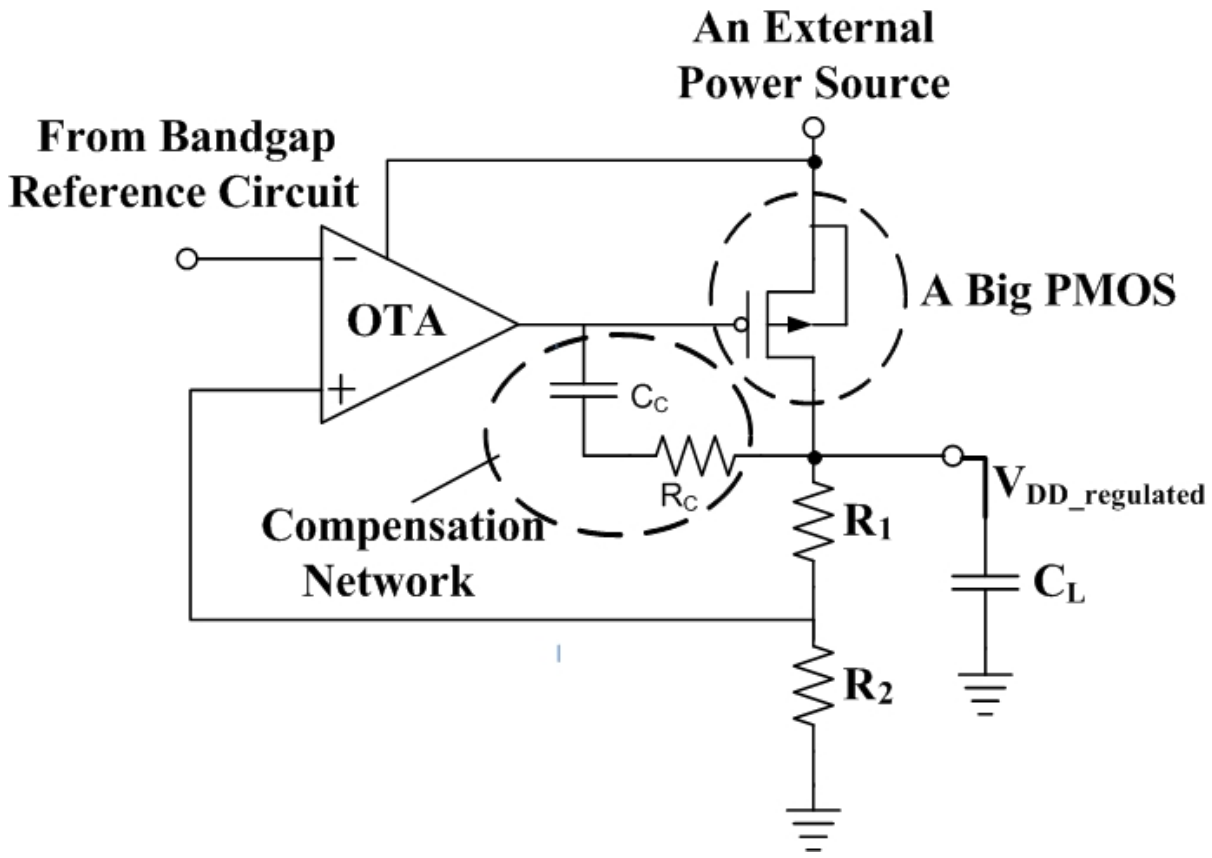


Fig. 3.24 Circuit diagram of a low voltage drop-out voltage regulator (LDO)

The regulated output voltage can be calculated as follows.

$$A_{V\_OTA} = \frac{R_2}{R_1 + R_2}, \tag{3.28}$$

$$V_{DD\_regulated} = \left(1 + \frac{R_1}{R_2}\right) V_{Bandgap} \tag{3.29}$$

In this LDO design, a large PMOS has been used because this regulator is supposed to provide a stable voltage, negative feedback for the system as well as a sufficient current for the entire signal processing block. Also, this large PMOS helps to achieve the desired low voltage drop at

the smallest supply voltage, which is an external power supply in this case, and for the maximum load current.

For the stable frequency response, the compensation network has been used in this LDO design. Choosing C_C and R_C for the compensation network requires the same procedure as the OTA design. However, there is one important thing to be considered, that is, a gate capacitance in the large PMOS. Since the W/L ratio of this PMOS is large, the gate capacitance is also significantly large as well. Thus, to calculate the value of C_C, and R_C, the gate capacitance of the large PMOS should be considered carefully. Furthermore, this low-dropout regulator is required to have a large C_L, which is connected to output, for a stable operation.

3.6 The Potentiostat Design

3.6.1 The Potentiostat

The potentiostat is one of the main functional blocks in this design. This function of this block is to bias a biosensor. A biosensor will produce a sensor current as long as the *work_electrode* (*Work_el*) and the *reference_electrode (Ref_el*) maintain a fixed voltage of 0.7V. The mechanism of producing sensor current for the signal processing unit is by maintaining 0.7V between the *work_electrode* and the *reference_electrode*, a positive and negative charges are created in a chemical solutions[7] which are gathered by the *collect_electrode (Collect_el*). Therefore, the *collect_electrode* produces the current for the signal processing circuit proportional to the concentration of the target analytes**.** Fig. 3.25 shows the detail of the potentiostat circuit diagram.

The operating principle of the potentiostat can be explained as follows. U1 through U4 are a set of operational amplifiers, which are the basic building blocks of the potentiostat. U1 and U2 work as buffers, U3 works as a unity gain differential amplifier and finally U4 works as an error amplifier. The potential difference of 0.7V from the voltage regulator sustains a stable reference voltage at the non-inverting terminal of the error amplifier. The output of the error amplifier is fed back to the *work_electrode* to compensate for any deviation from 0.7V voltage difference between the *work_electrode* and the *reference_electrode*. The equation as shown below if obtained by applying the KCL at the inverting terminal of U3[7].

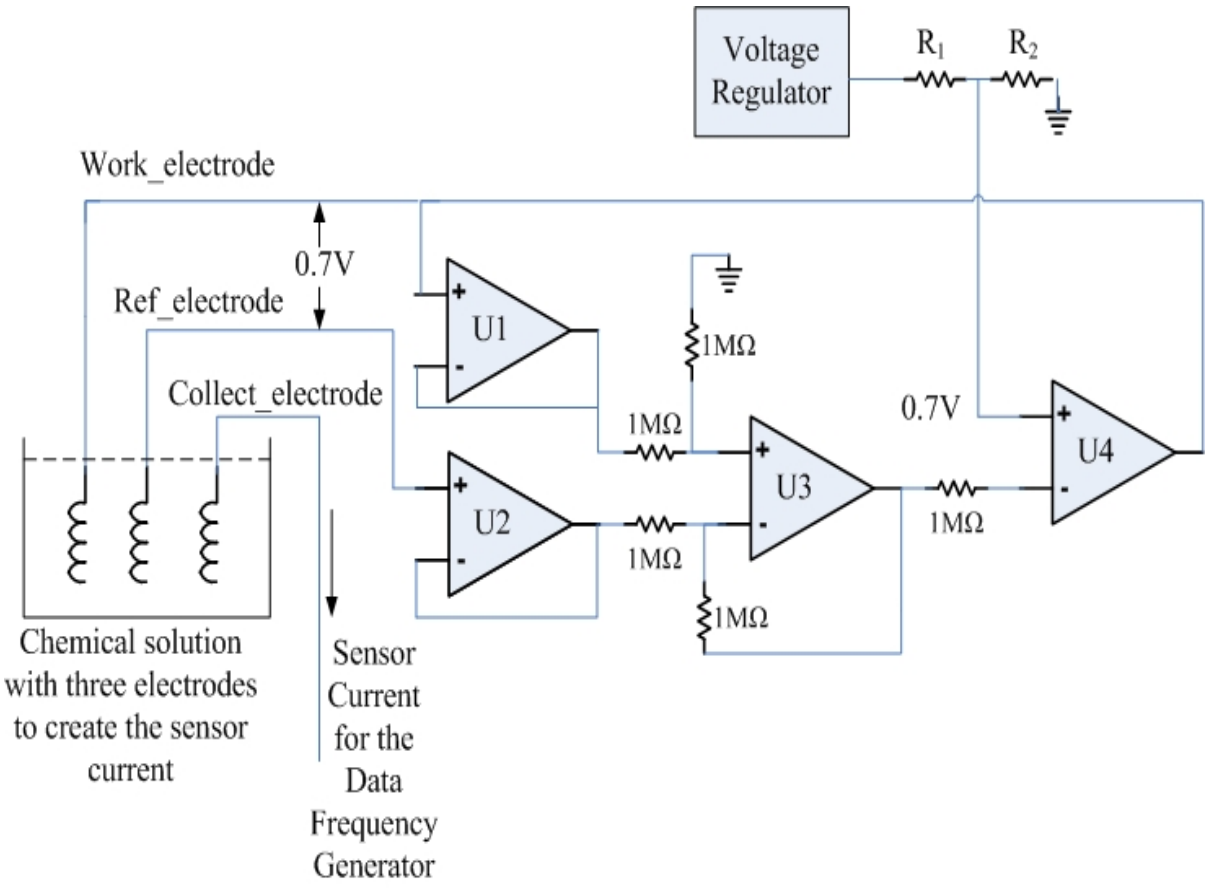


Fig. 3.25 Block diagram of the potentiostat circuit

$$V_{ref\_el} - \frac{V_{work\_el}}{2} = \frac{V_{work\_el}}{2} - 0.7$$
$$\therefore V_{work\_el} - V_{ref\_el} = 0.7 \tag{3.30}$$

where, $V_{reference}$ and $V_{work\_electrode}$ are the potential of reference and work electrodes.

Also, all the amplifiers are assumed to be as ideal amplifiers. Operational amplifiers, U1 through U4 are explained early section. These set of operational amplifiers are not the OTA since these op-amps should be able to drive resistive loads. So, Op-Amps in the potentiostat are a two-stage operational amplifier with output buffer. Detail of the operational amplifiers can be found in early section.

3.7 The Complete System

Fig. 3.25 shows the entire system of FSK modulation.

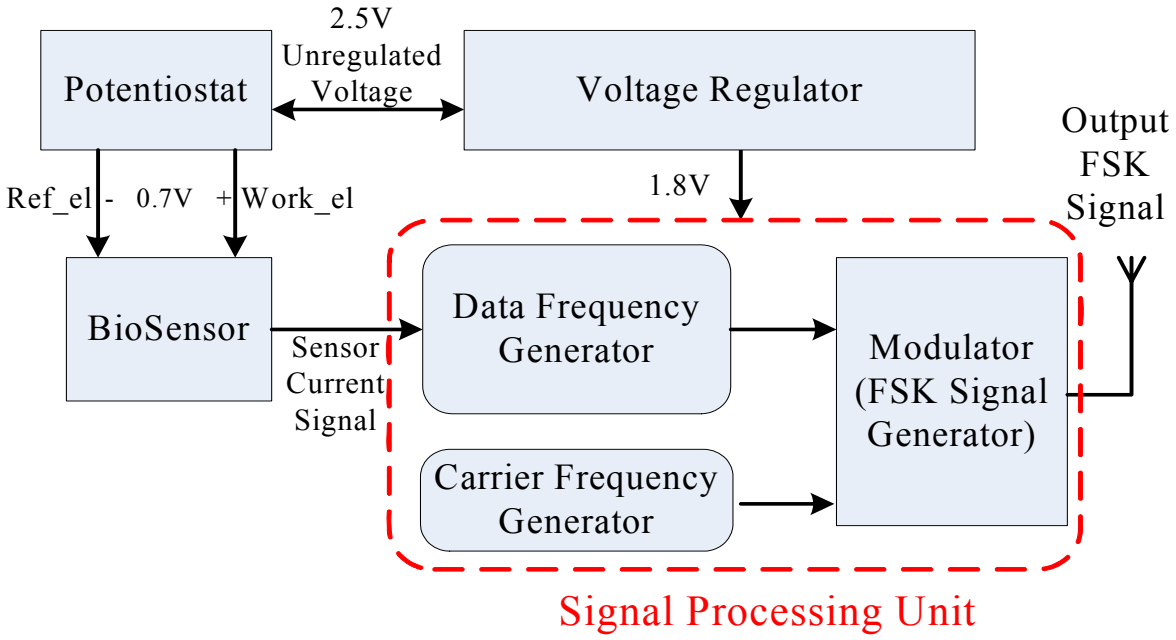


Fig. 3.26 Block diagram of the complete system

The unregulated voltage of 2.5V will be generated from the wireless inductive link, which has been discussed in chapter 1. This 2.5V will power up the potentiostat as well as the voltage regulator. The regulated voltage of 1.8V, which comes from the voltage regulator will power up the signal-processing unit. The FSK modulated signal will be transmitted to outside via a wireless system using inductive link. The current levels, which come from the biosensor will be in the range of 0.2uA to 2uA. The data frequency generated by the sensor current will be proportional to the range of the input currents. The detailed simulation and test result will be presented in the next chapter.

Chapter 4
LAYOUT, ACTUAL SCHEMATICS, SIMULATIONS, AND TEST RESULTS

4.1 Layout

In this section, the layout techniques as well as the actual layout of the chip is presented. The process chosen for this design is AMI 0.5-μm CMOS process due to its low cost as well as maturity. The entire circuit has been built and laid out by using Cadence. DRC (design rules check) and LVS (layout vs. schematic) have been used to verify the layout.

4.1.1 Matching Layout Techniques of CMOS Transistors

Most CMOS analog integrated circuits heavily rely on matching rather than the absolute values. Because of process variation during manufacturing, parameters can vary as much as ± 20%[25]. For instance, the differential input pairs require the matching of gate-to-source voltages, and the current mirrors depend on the matching of the drain currents. The matching is affected by sizes as well as the shapes of the CMOS transistors. Usually, large size of transistors match better than small sizes because long channel transistors match better than short one by minimizing the channel length modulation. Also, transistors laid out in the same orientation will give better matching due to the transconductance, which depends on the carrier mobility. Diffusion and etching will hurt the matching of transistors. To prevent such events, using a dummy gate as shown in Fig. 4.1 will be required.

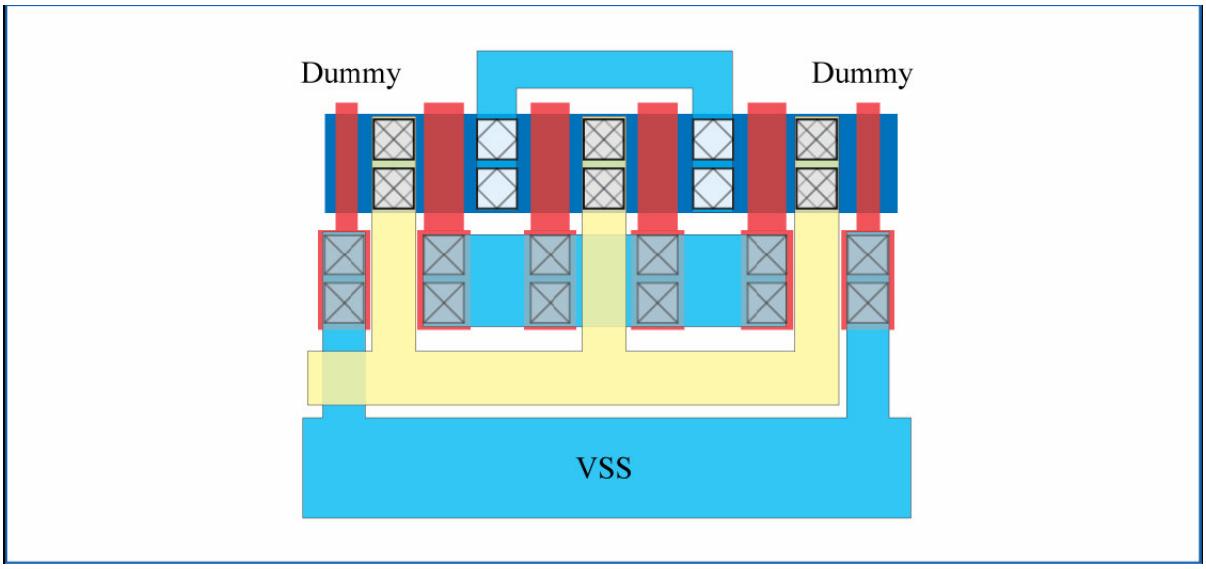


Fig. 4.1 Layout example of a dummy gate

4.1.2 Rules of CMOS Transistor Matching

Some of the most important layout rules of the matching of CMOS transistors[25] are summarized below.

- Place the transistors in the same direction and as close as possible. Parallel and close transistors help to reduce variations of transconductance.
- Use identical fingers for all matched transistors.
- Use dummy gates to minimize the effects of etching.
- Use the common-centriod layout techniques. The matched transistors should be equally separated into even number of fingers and laid out symmetrically.

4.1.3 Layout of the Actual Chip

The layout of the complete chip is shown in Fig. 4.2. The entire size including pad of laid out region is 1500μm × 1500μm, and actual area that has been use for the chip layout is about 1000μm × 1000μm. Fig. 4.2 shows the actual picture of laid out for the entire circuit.

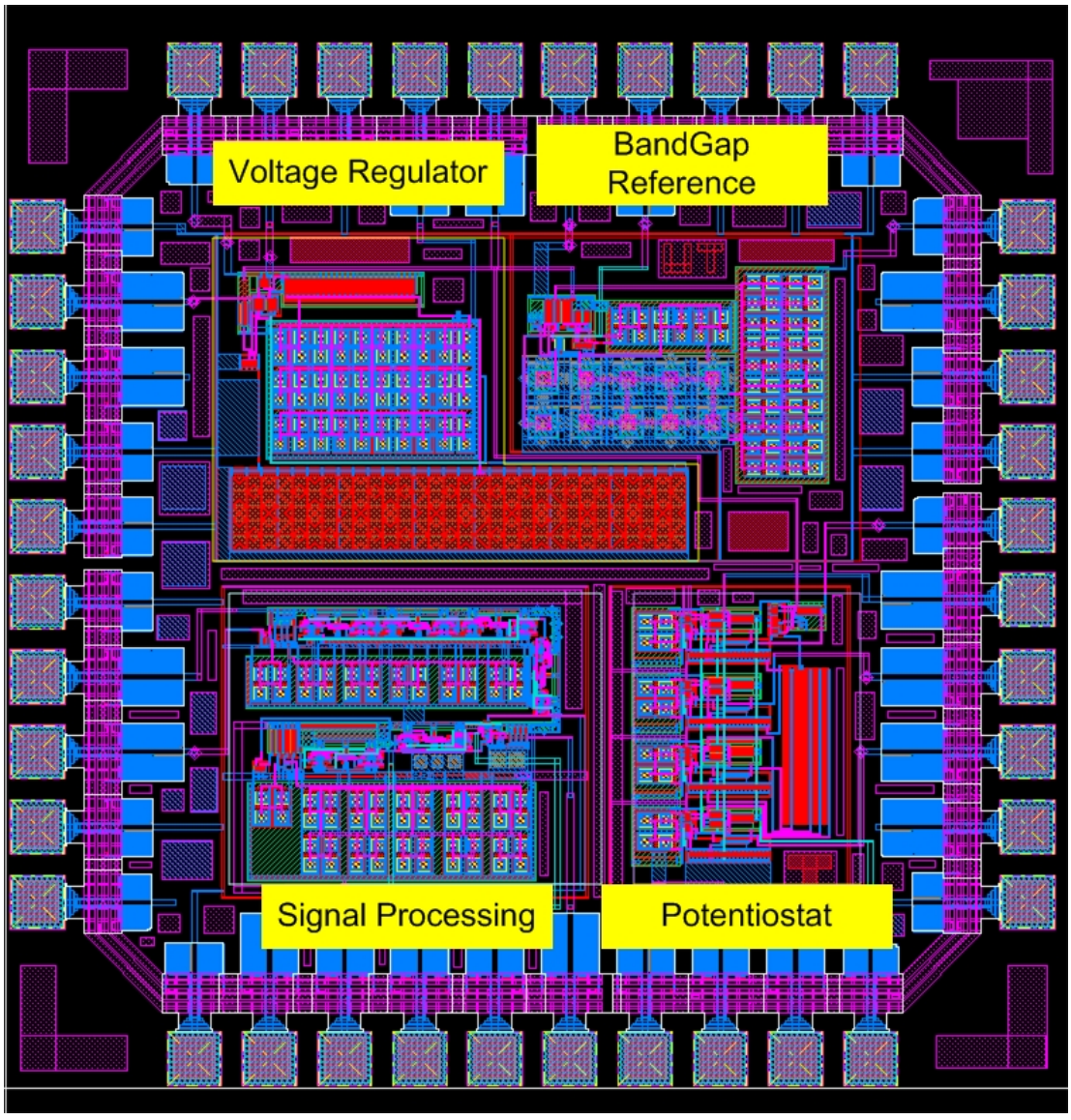


Fig. 4.2 Layout of the complete circuit

4.2 Actual Schematics

In this section, the actual schematics that have been used to simulate and to layout the complete circuit is presented. Fig. 4.3 through 4.12 show the building blocks of the complete FSK modulator circuits

4.2.1 Current Controlled Oscillator (CCO) –Data Frequency Generator

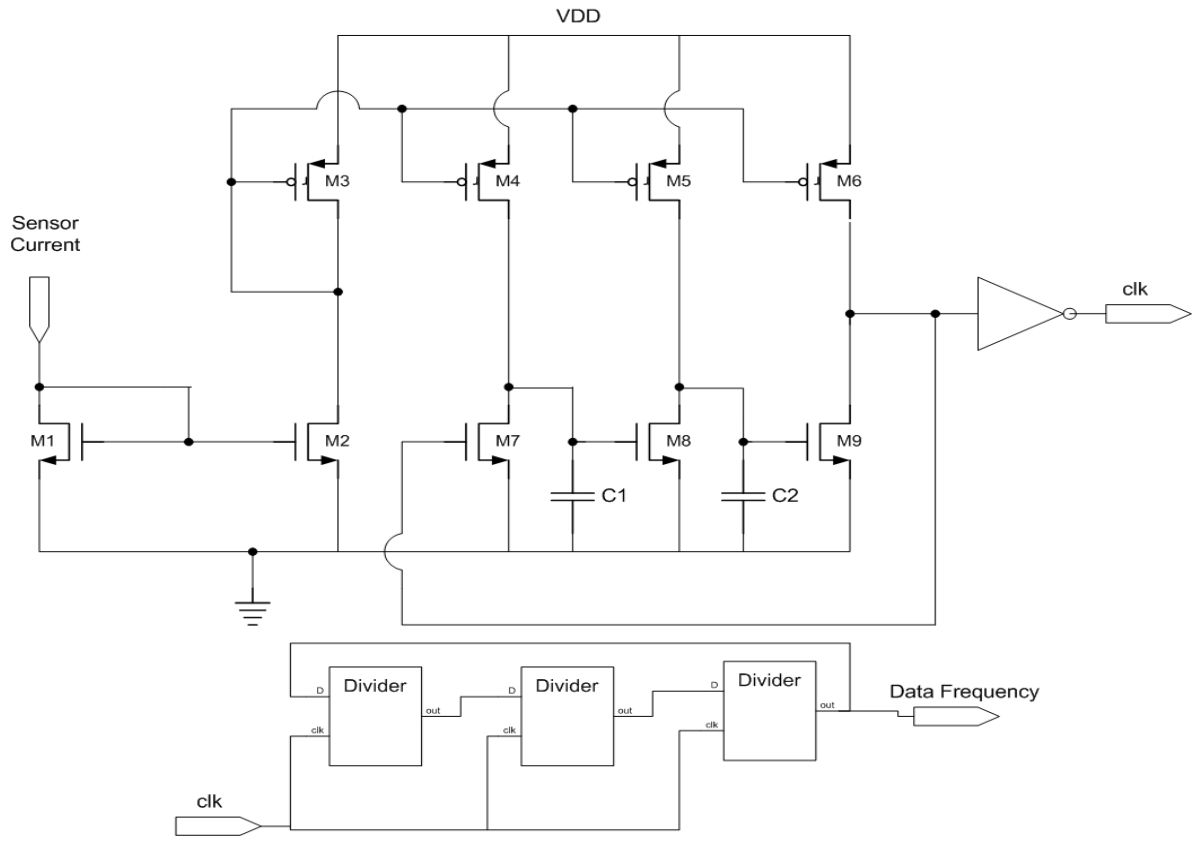


Fig. 4.3 Circuit diagram of CCO-data frequency generator

4.2.2 Current Controlled Oscillator (CCO) –Carrier Frequency Generator

Fig. 4.4 shows the actual schematic of carrier frequency generator. The only difference between data frequency generator and carrier frequency generator is whether it uses the resistor or not. Since the carrier frequency generator has to generate a fixed frequency, CCO for the carrier frequency generator uses a resistor.

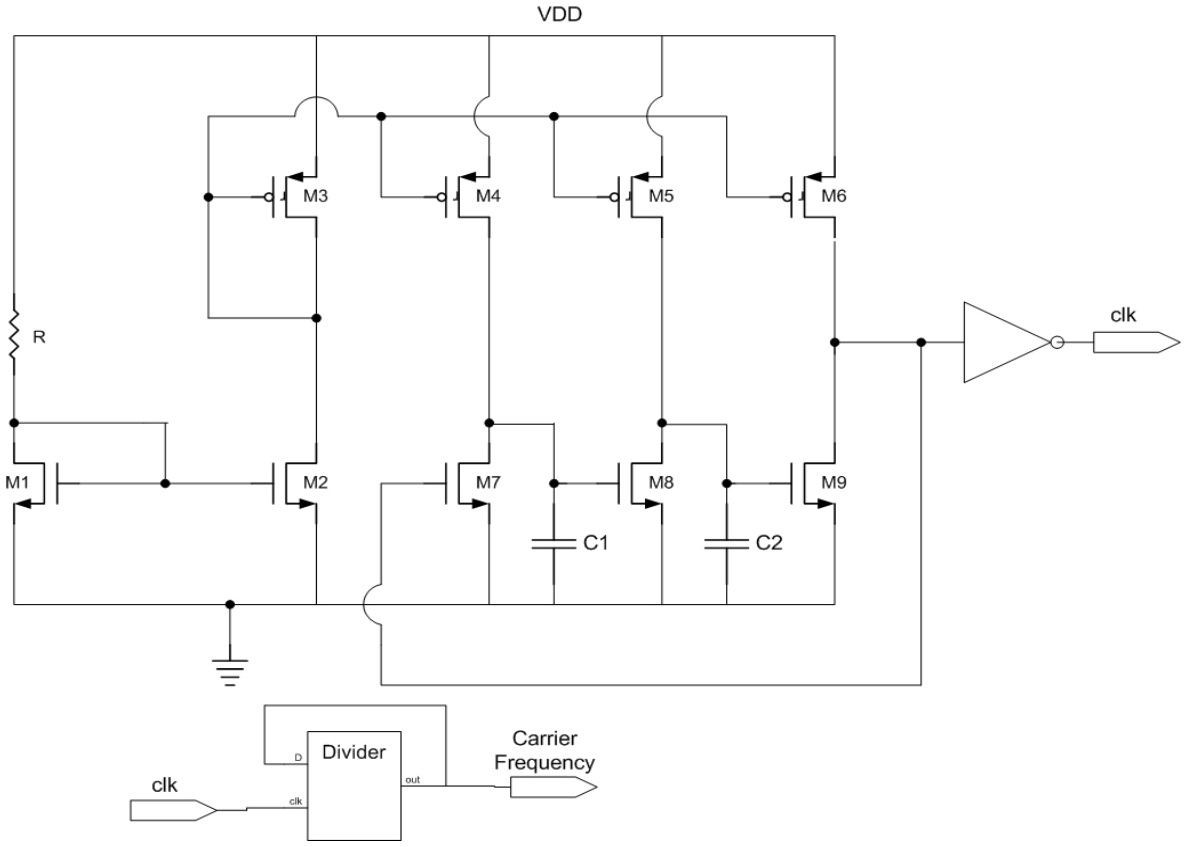


Fig. 4.4 Circuit diagram of CCO-carrier frequency generator

4.2.3 D-Latch

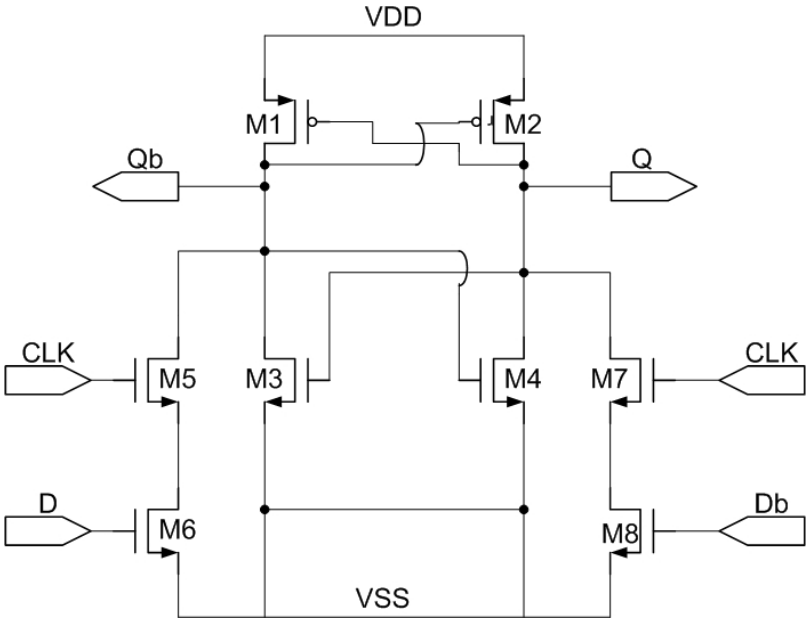


Fig. 4.5 Circuit diagram of the D-latch

4.2.4 Operational Amplifier and Op-Amp with Buffer

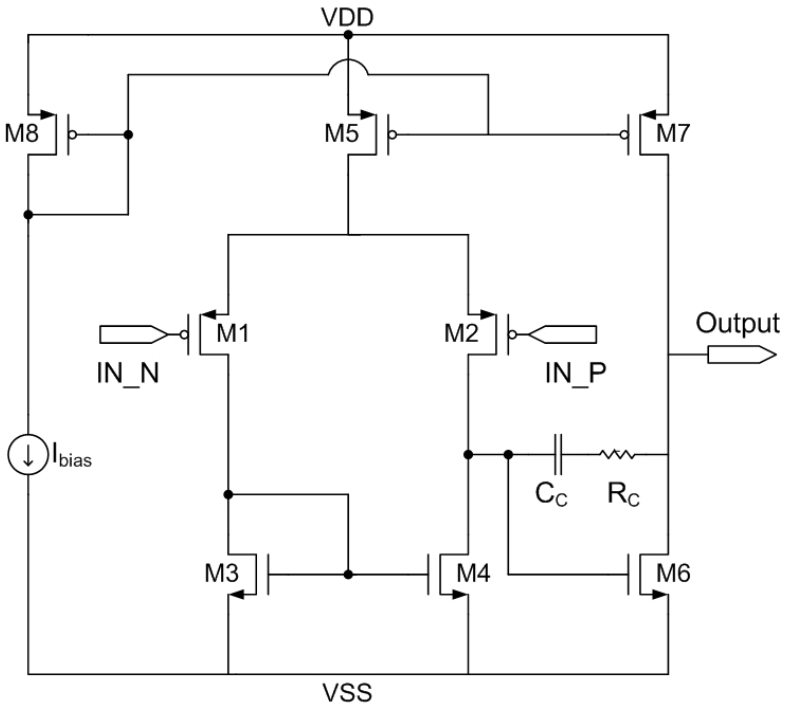


Fig. 4.6 Circuit diagram of the operational amplifier

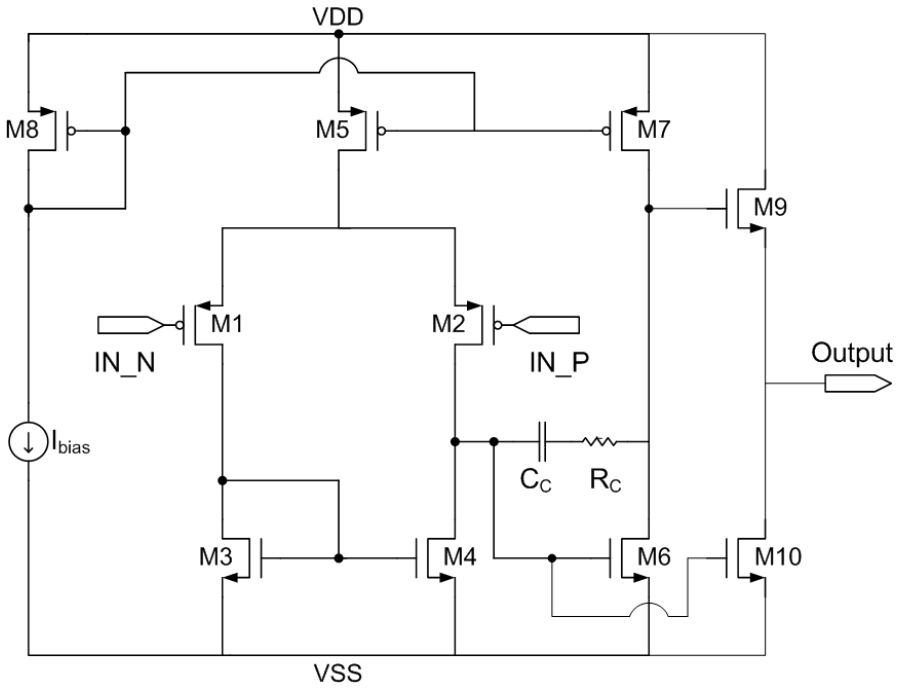


Fig. 4.7 Circuit diagram of the operational amplifier with buffer

4.2.5 Bandgap Reference

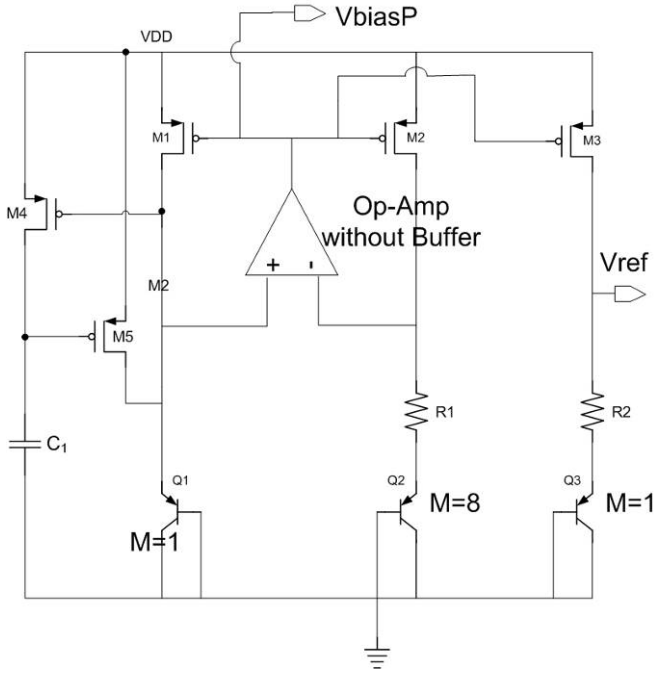


Fig. 4.8 Circuit diagram of the bandgap reference

4.2.6 Voltage Regulator

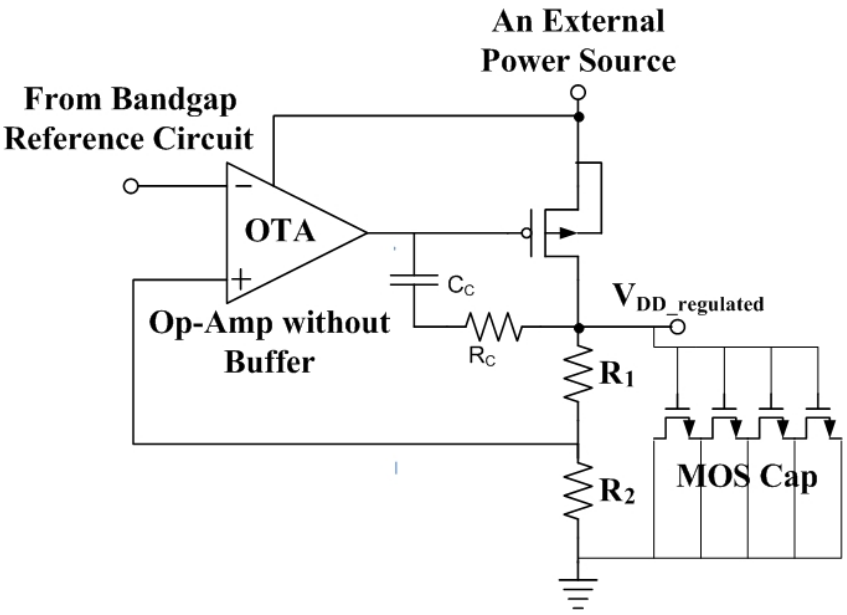


Fig. 4.9 Circuit diagram of the voltage regulator

4.2.7 Signal Processing

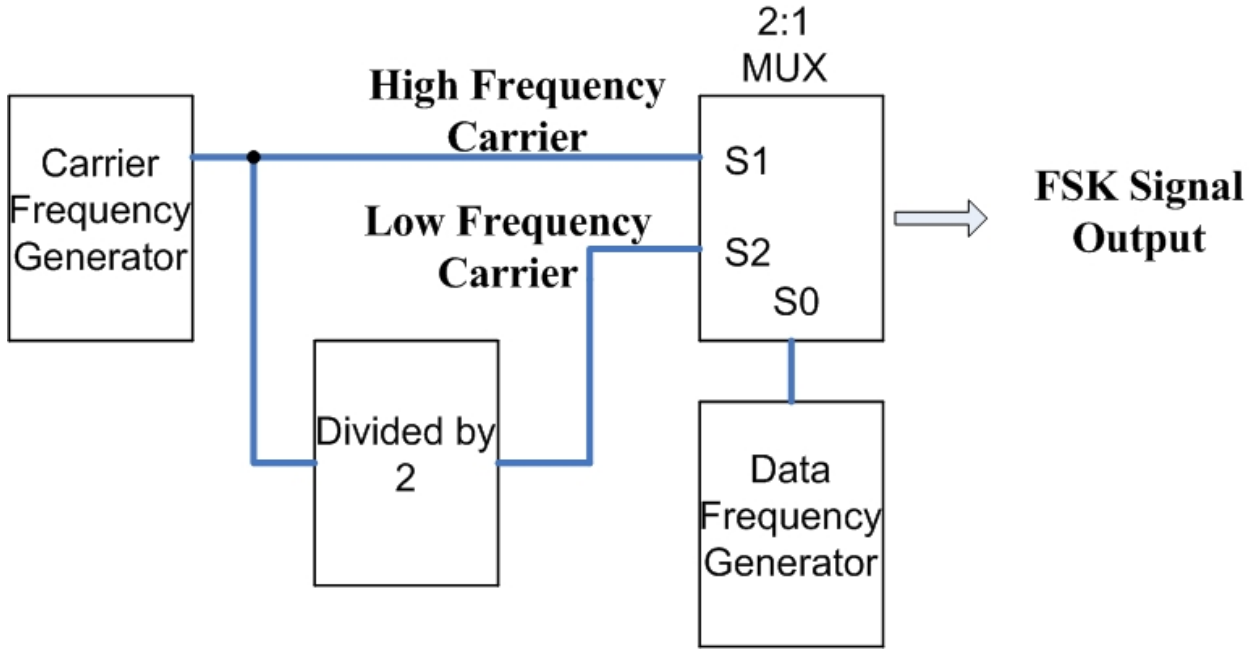


Fig. 4.10 Block diagram of the signal processing unit

4.2.8 Potentiostat

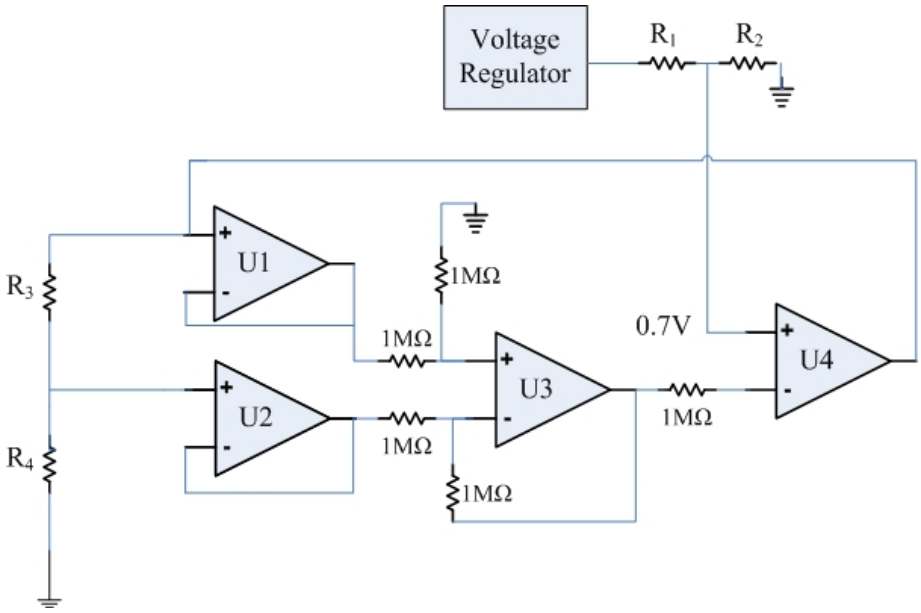


Fig. 4.11 Circuit diagram of the potentiostat

4.2.9 The Complete Circuit

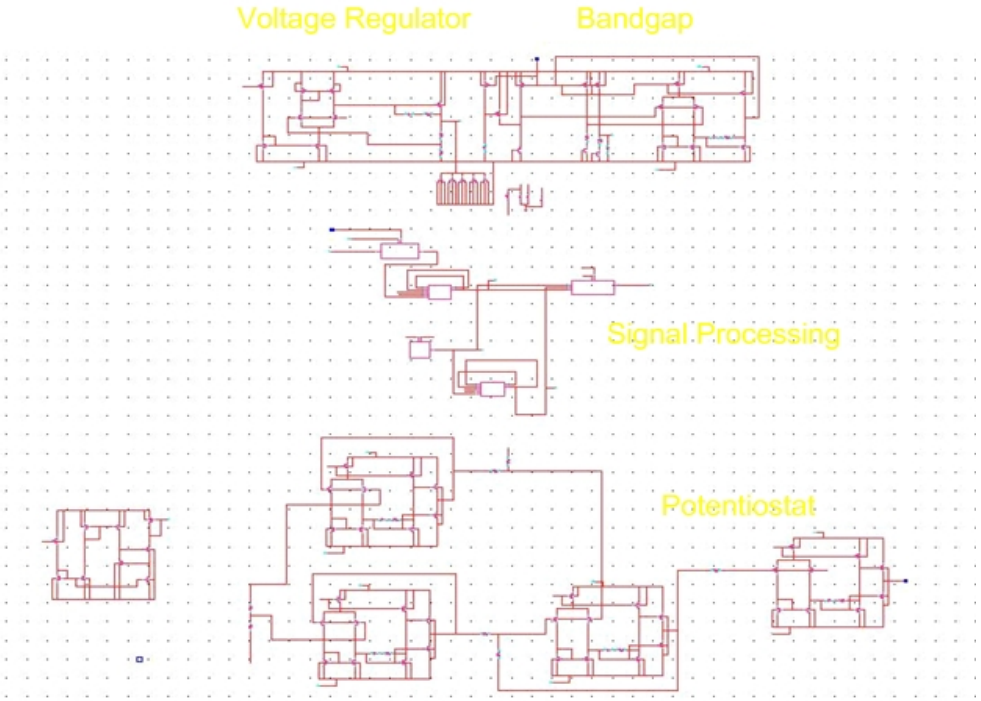


Fig. 4.12 Circuit diagram of the entire circuit diagram

4.3 Simulation and Test Results

In this section, simulation and test results of FSK modulator has been presented. Fig.4.13 through Fig.4.22 shows the simulation results and Fig.23 through Fig.32 shows the test results of FSK modulator.

4.3.1 FSK Signal, Data and Carrier Frequency

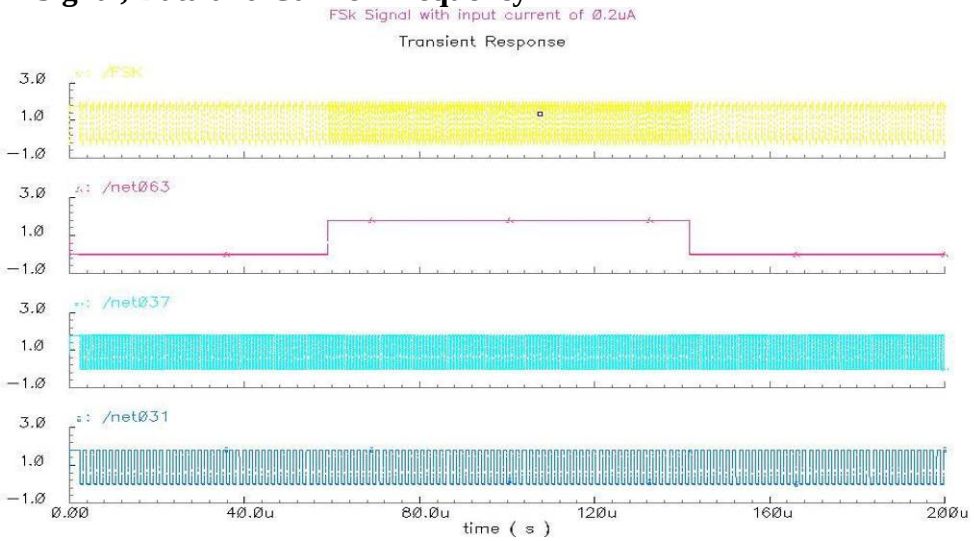


Fig. 4.13 FSK modulator simulation result when the input current is 0.2uA

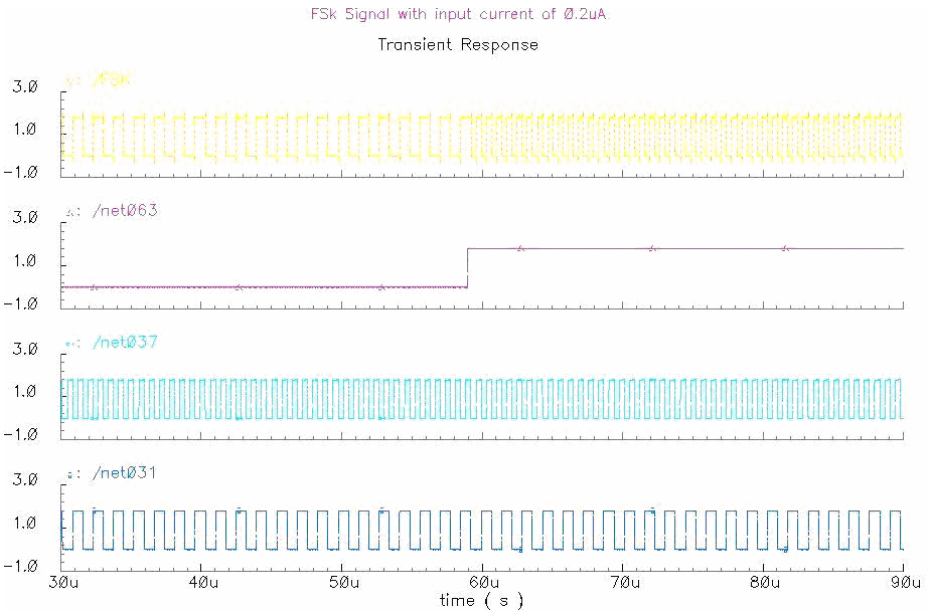


Fig. 4.14 FSK modulator simulation result when the input current is 0.2uA (Magnified Picture)

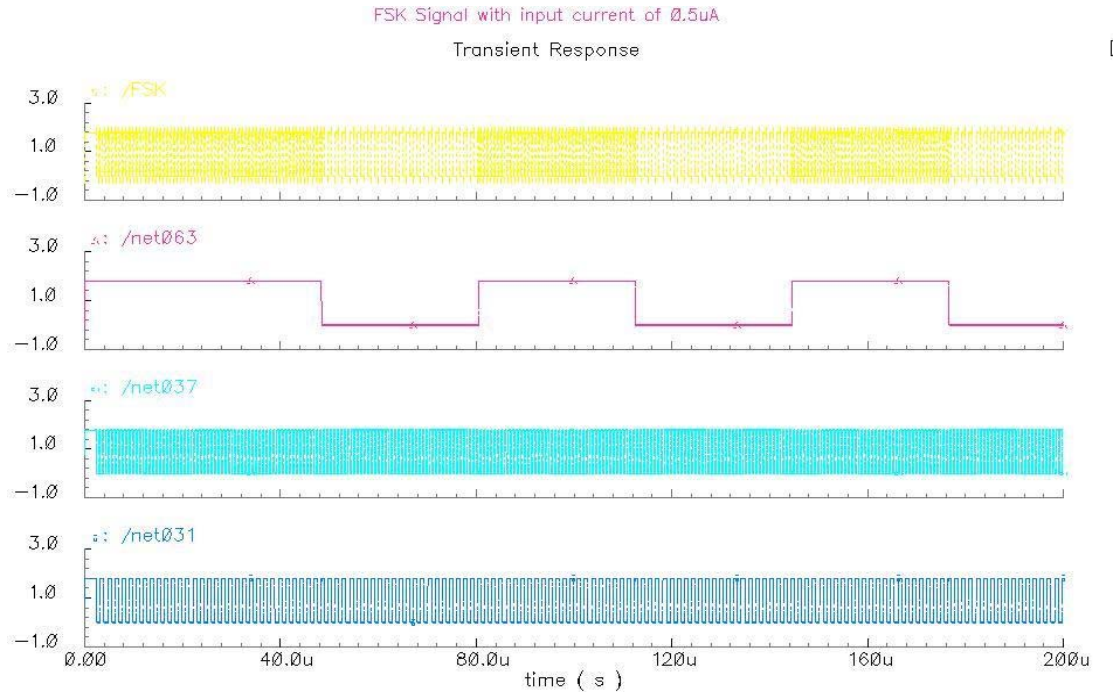


Fig. 4.15 FSK modulator simulation result when the input current is 0.5uA

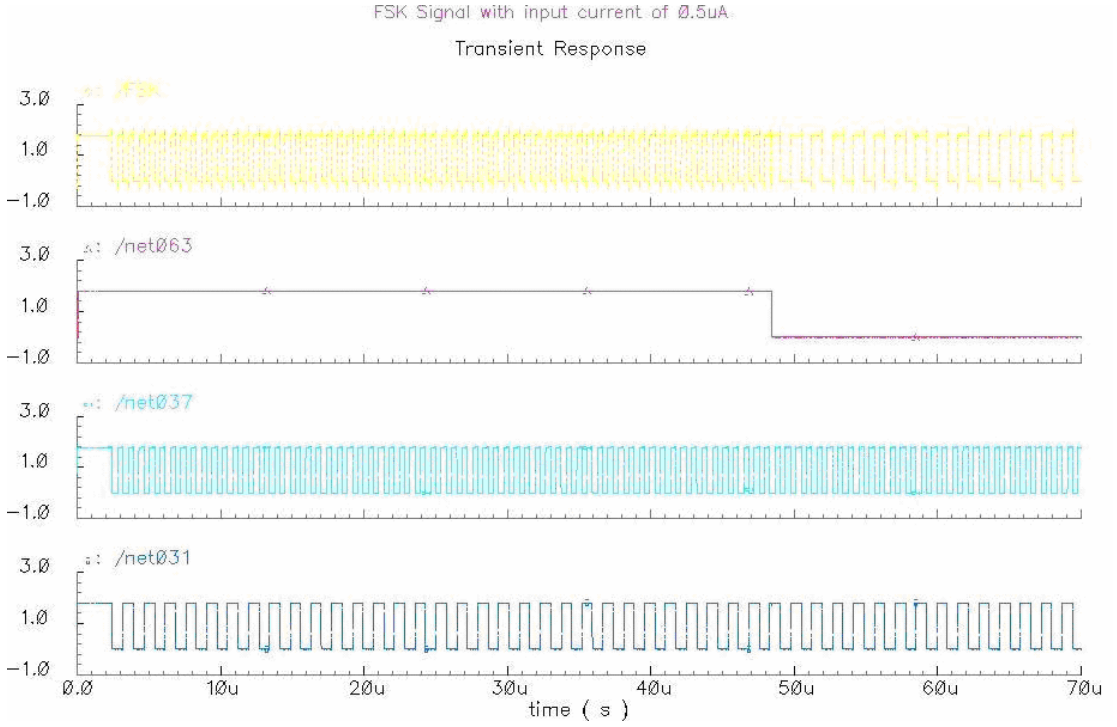


Fig. 4.16 FSK modulator simulation result when the input current is 0.5uA (Magnified Picture)

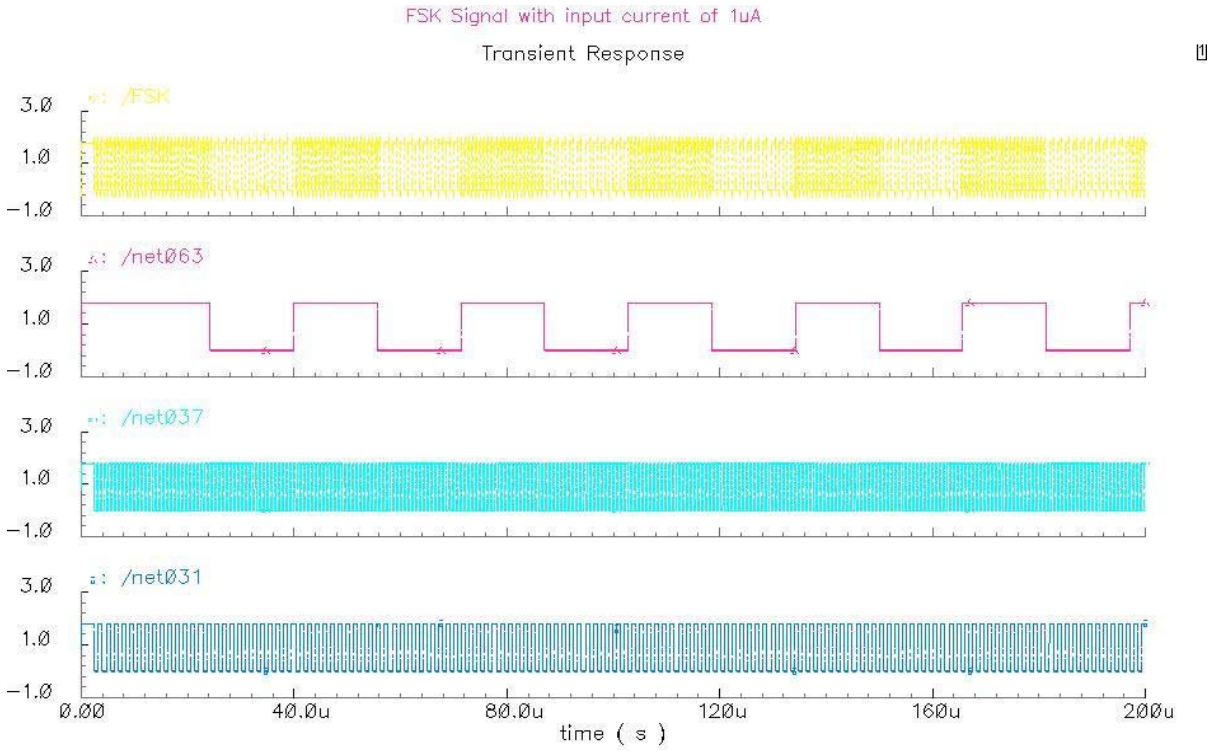


Fig. 4.17 FSK modulator simulation result when the input current is 1uA

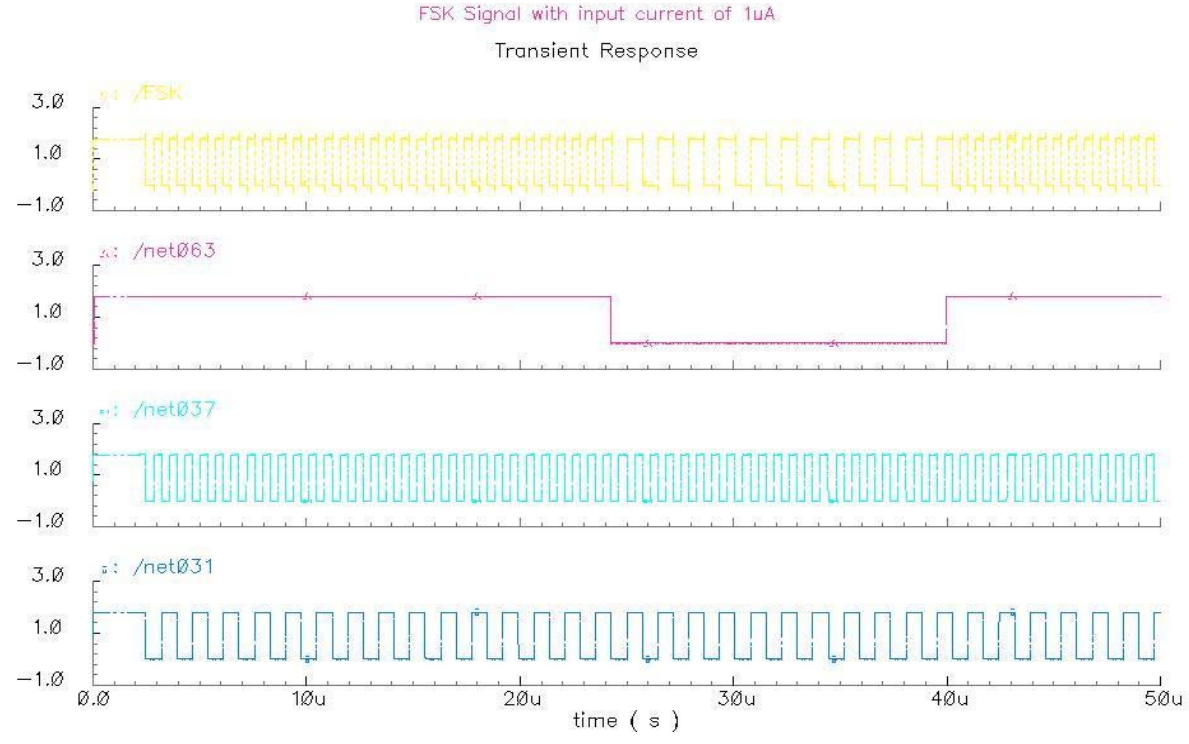


Fig. 4.18 FSK modulator simulation result when the input current is 1uA (Magnified Picture)

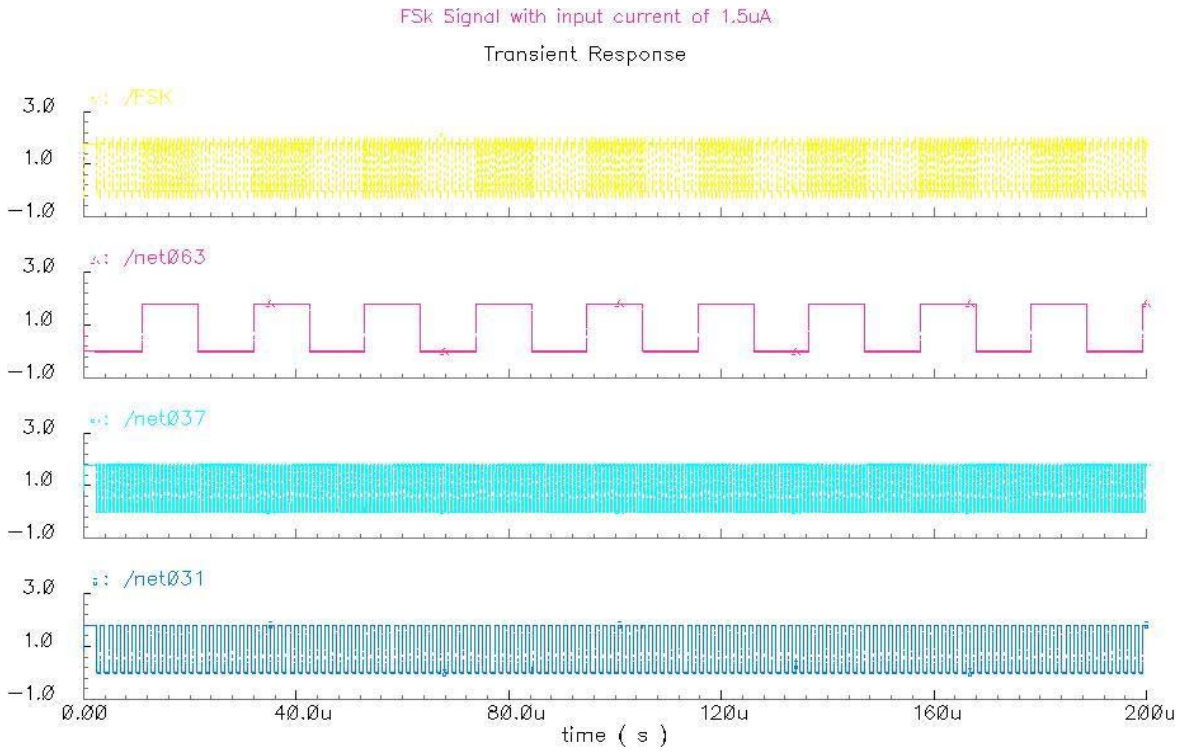


Fig. 4.19 FSK modulator simulation result when the input current is 1.5uA

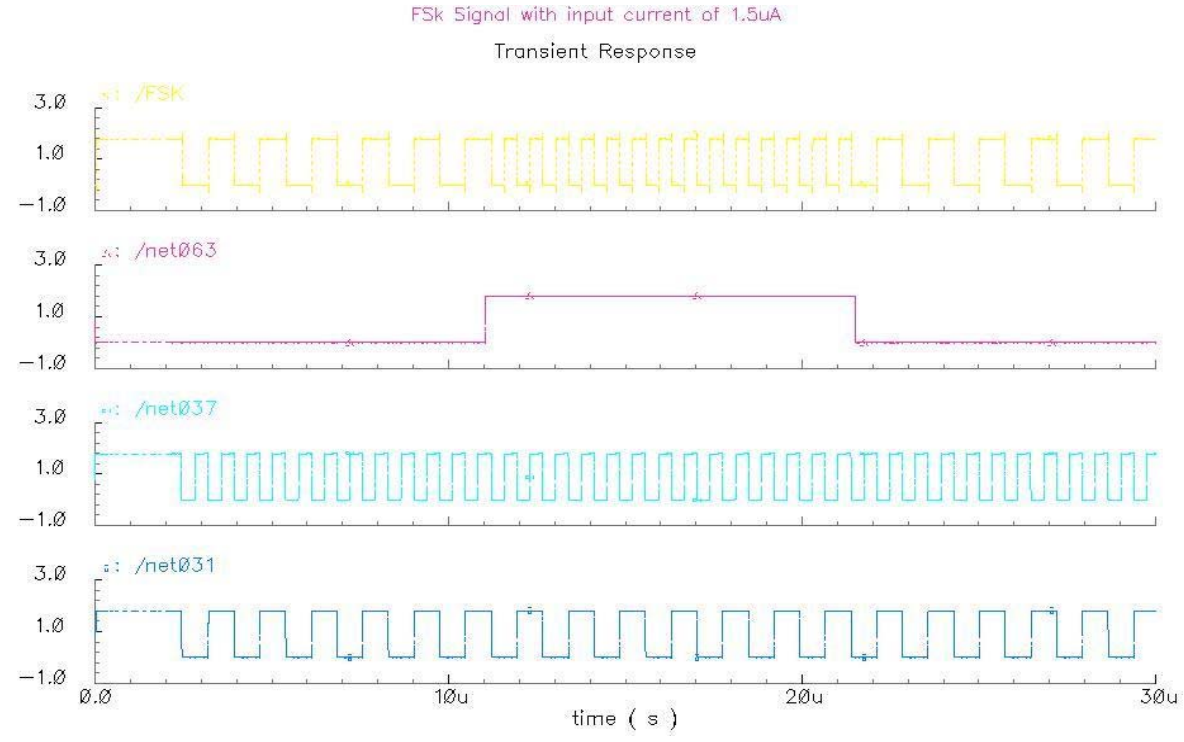


Fig.4.20 FSK modulator simulation result when the input current is 1.5uA (Magnified Picture)

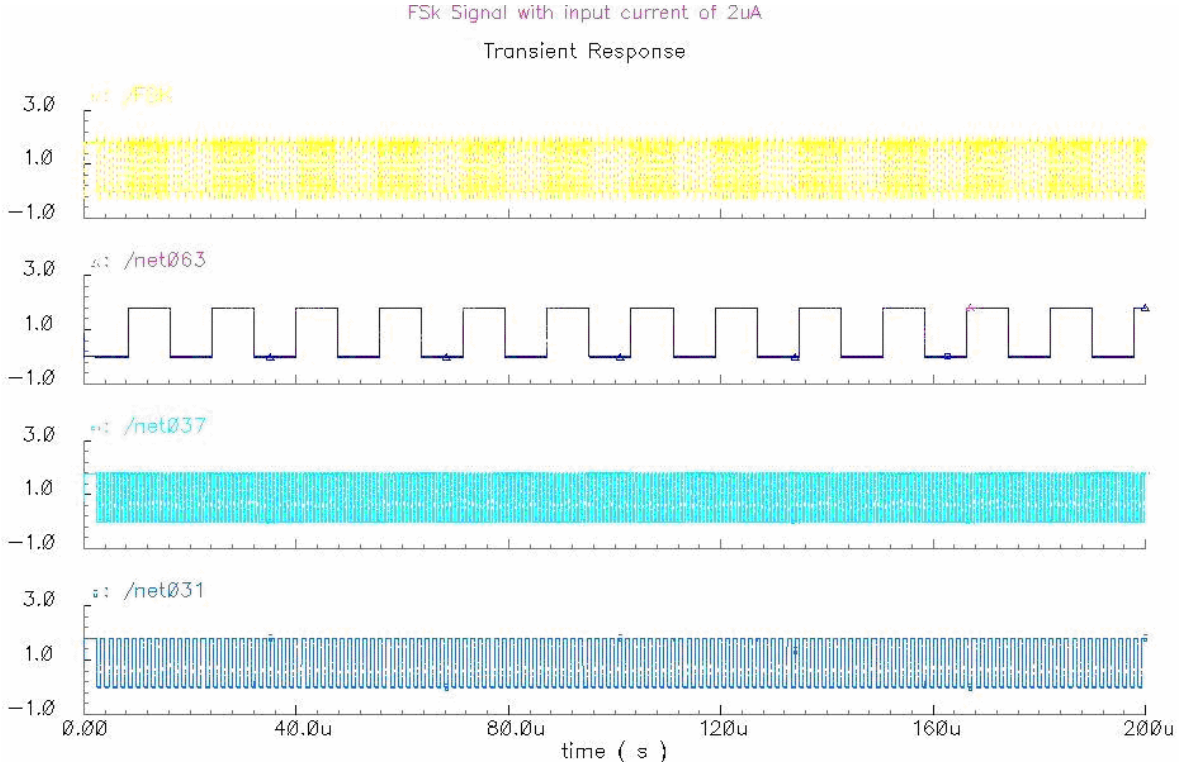


Fig.4.21 FSK modulator simulation result when the input current is of 2uA

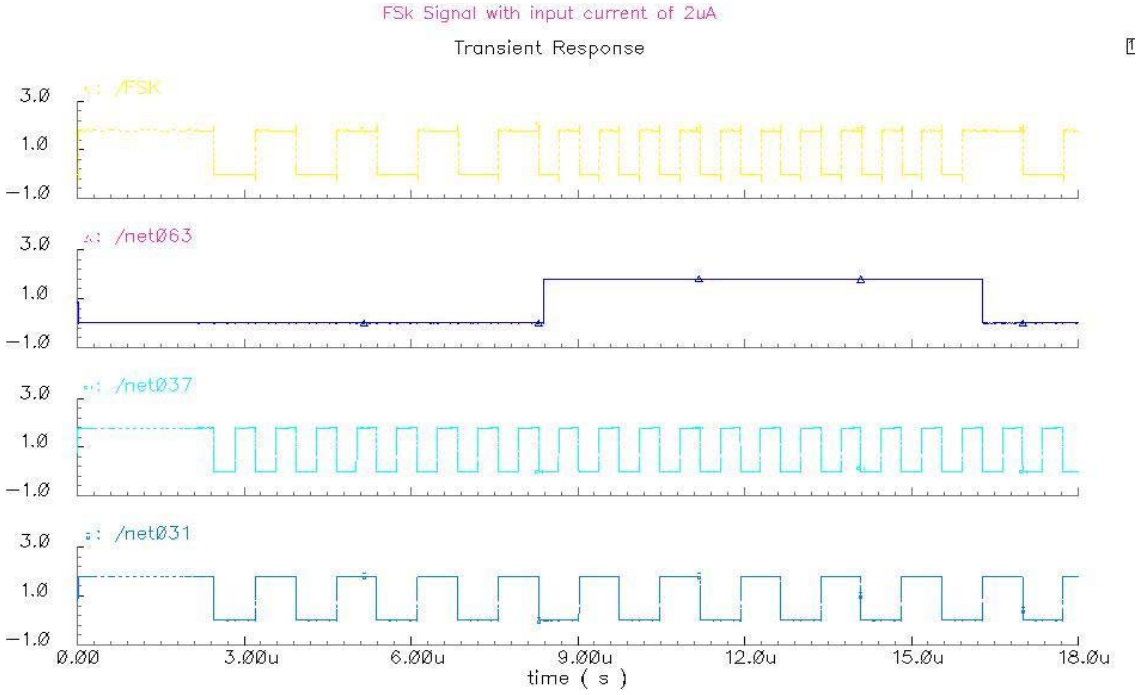


Fig.4.22 FSK modulator simulation result when the input current is 2uA (Magnified Picture)

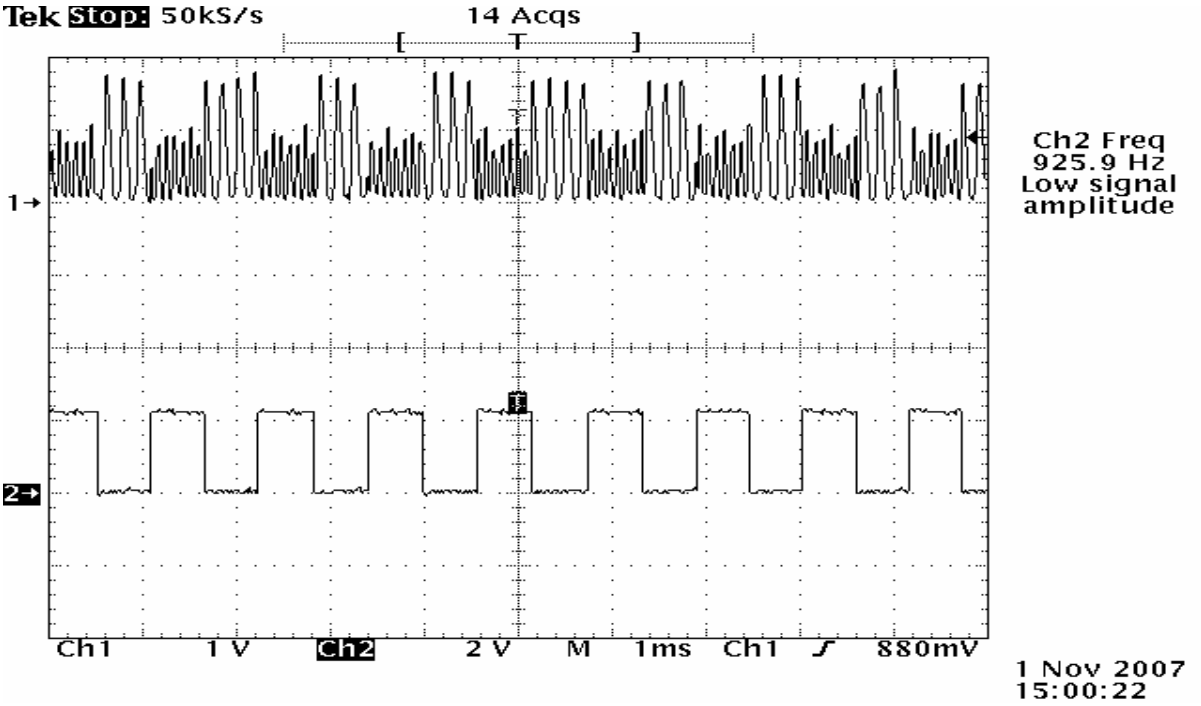


Fig.4.23 FSK modulator test result when the input current is 0.2uA

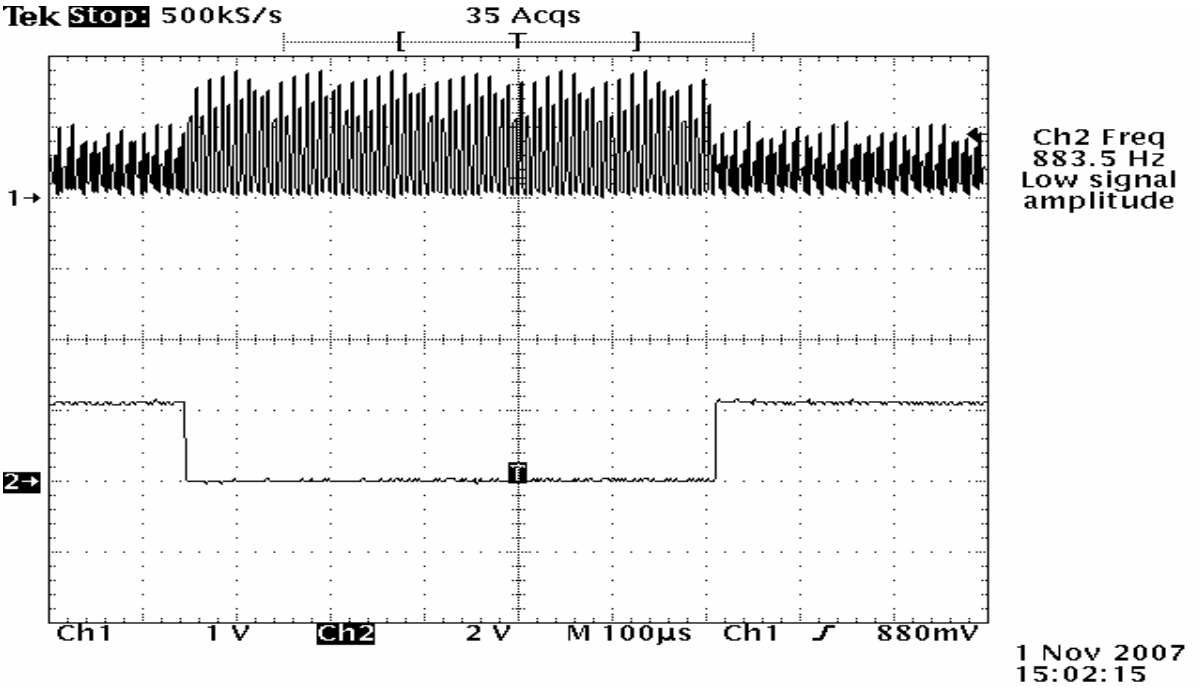


Fig.4.24 FSK modulator test result when the input current is 0.2uA (Magnified)

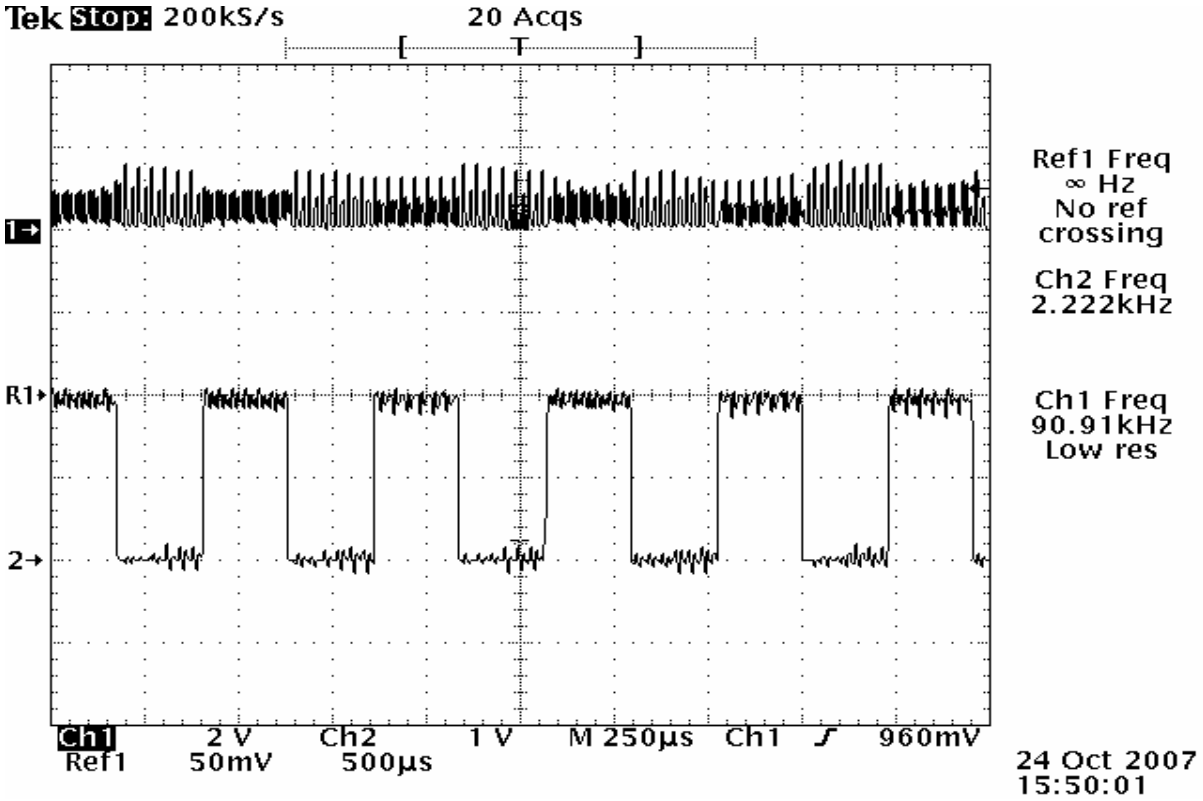


Fig.4.25 FSK modulator test result when the input current is 0.5uA

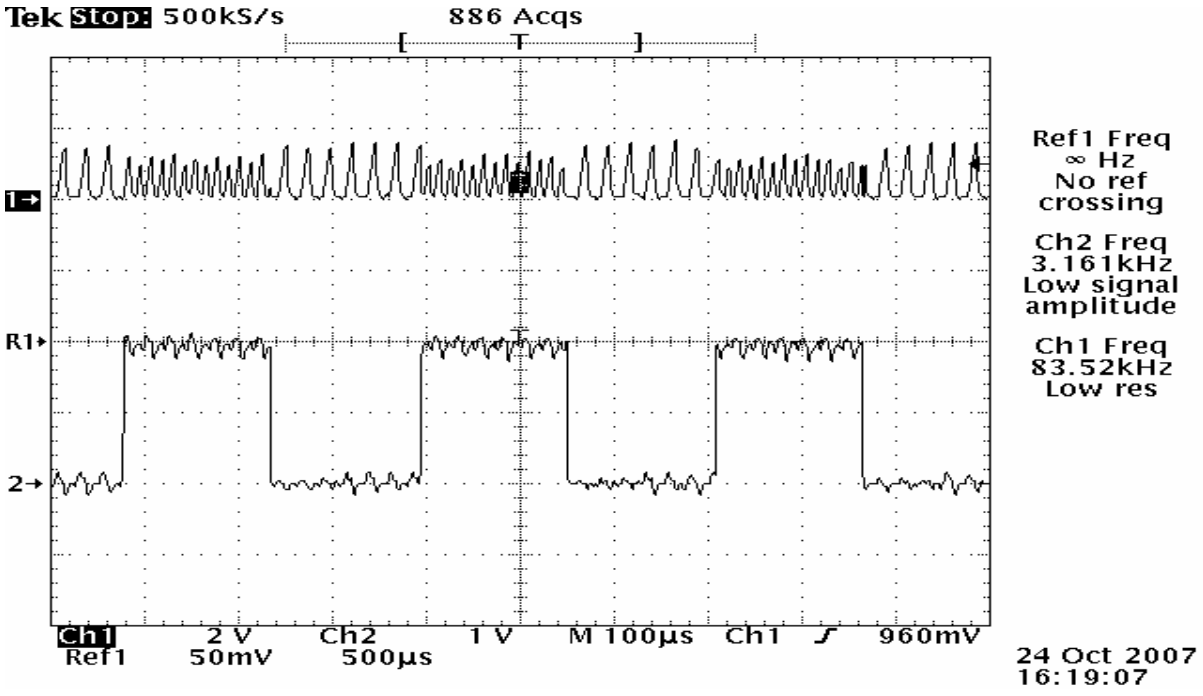


Fig.4.26 FSK modulator test result when the input current is 0.7uA

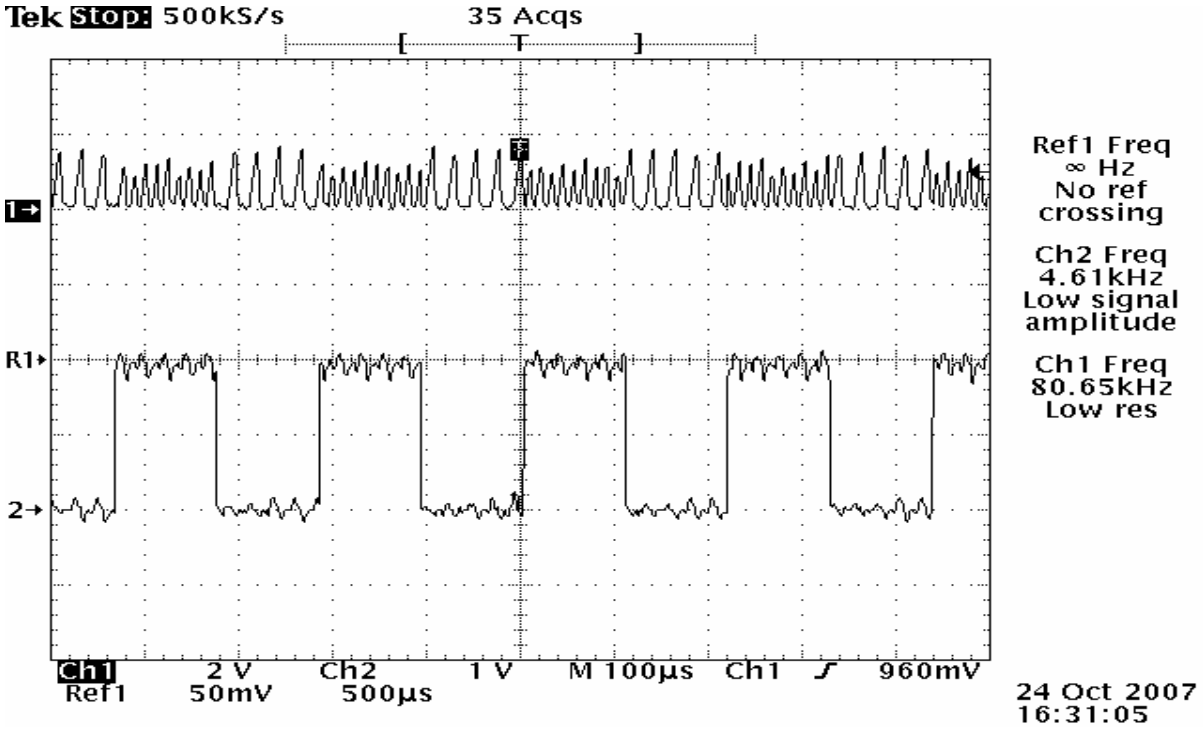


Fig.4.27 FSK modulator test result when the input current is 1uA

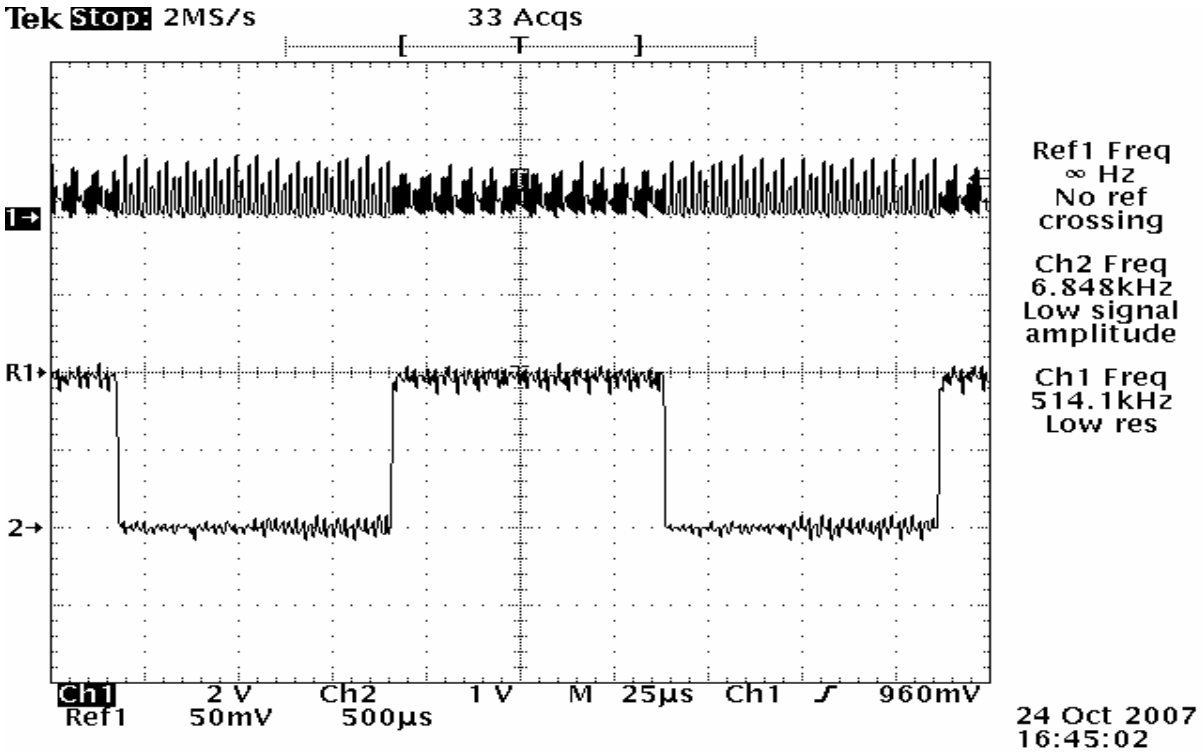


Fig.4.28 FSK modulator test result when the input current is1.5uA

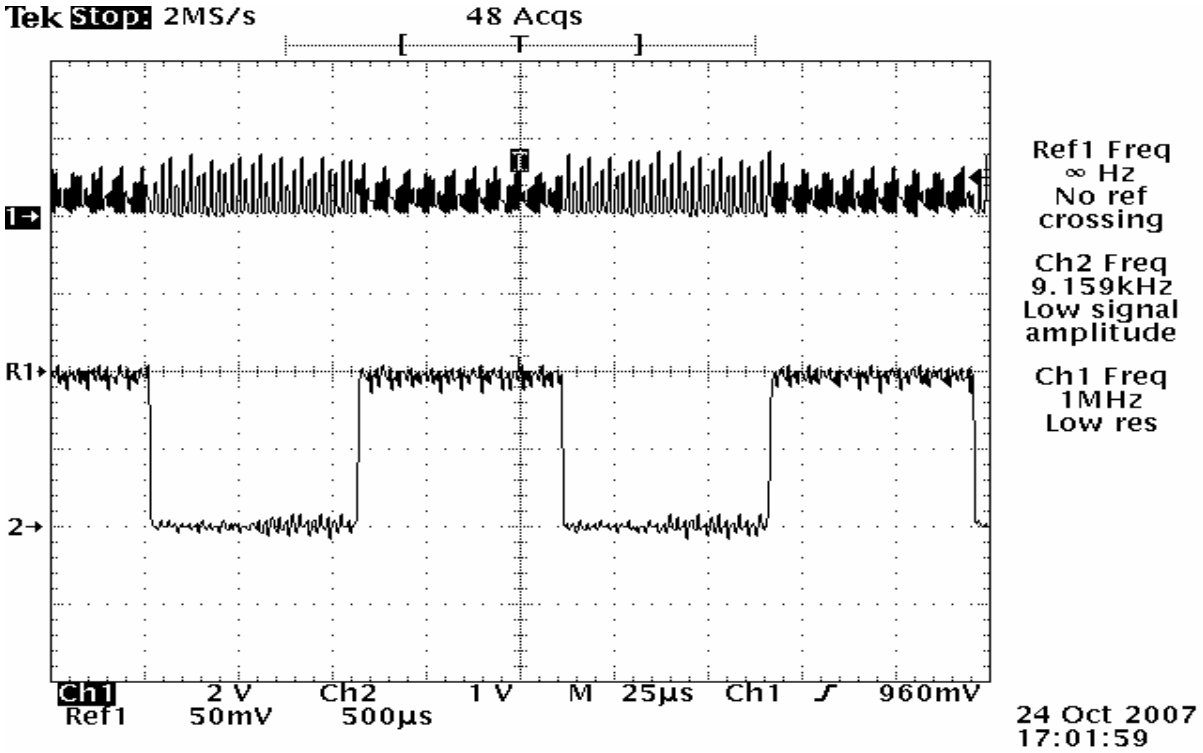


Fig.4.29 FSK modulator test result when the input current is 2uA

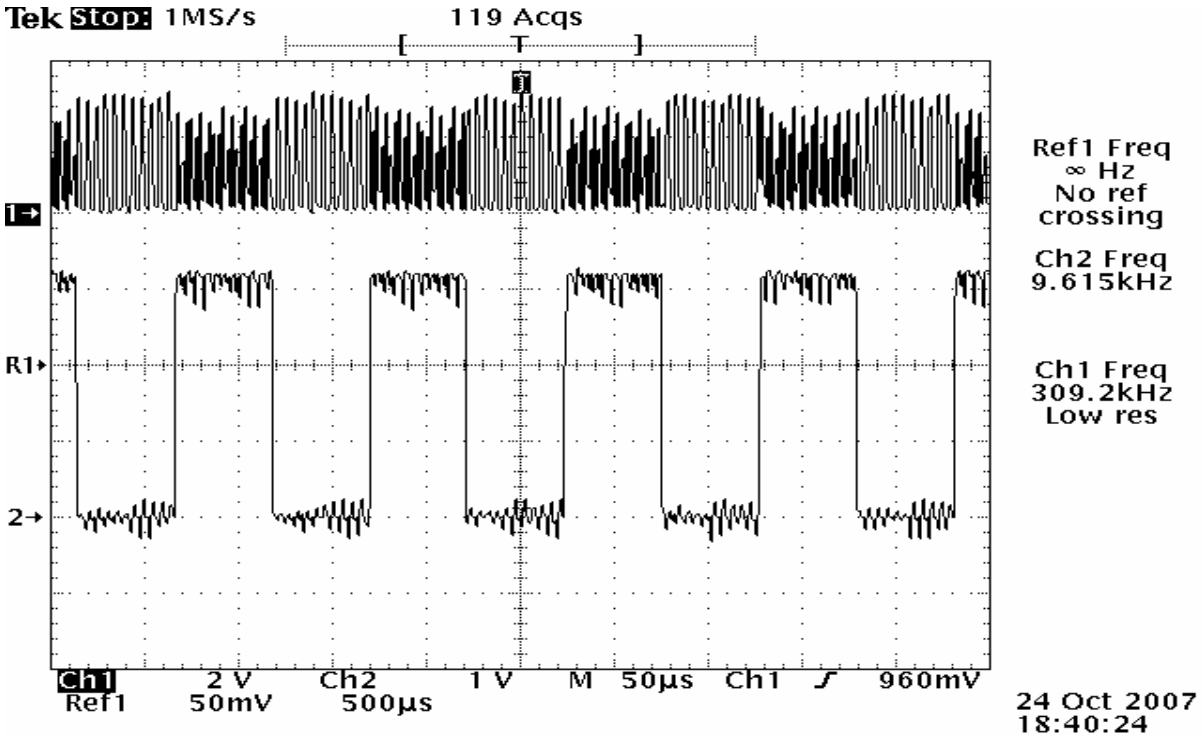


Fig.4.30 FSK modulator test result when the input current is 2uA with V_{DD} of 3.0V

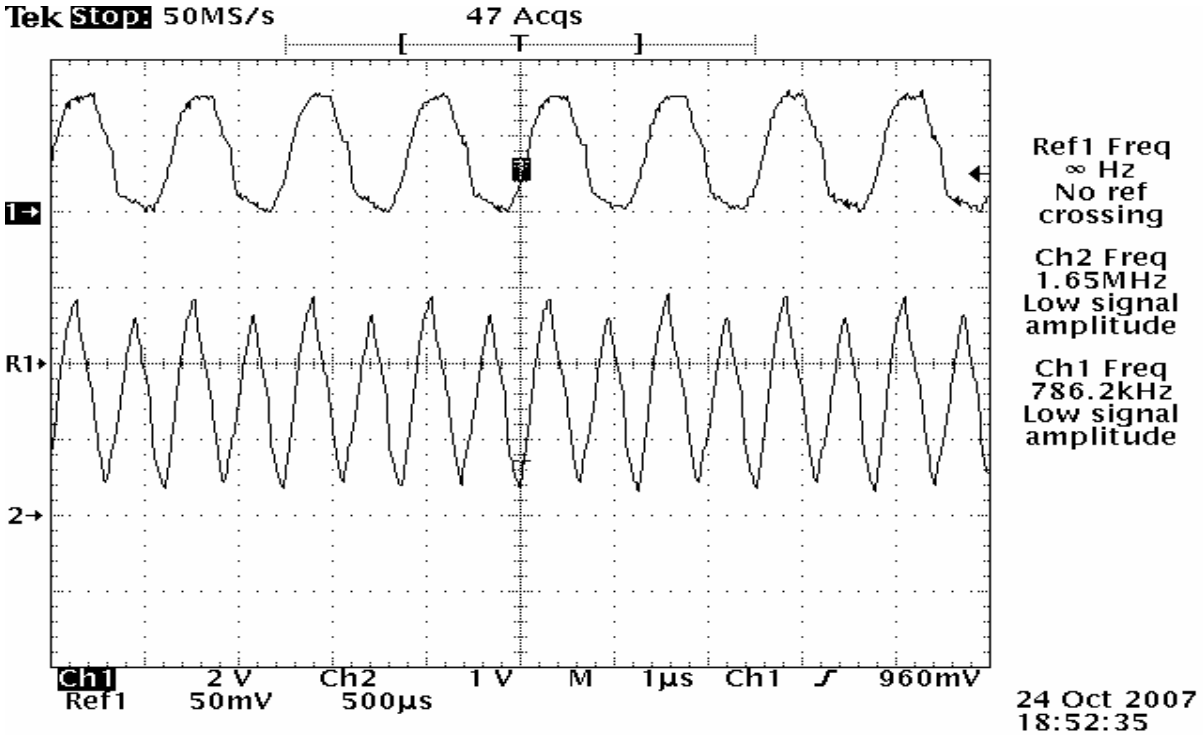


Fig.4.31 Test result of high and low carrier when V_{DD} is 3.0V and input current is 2uA

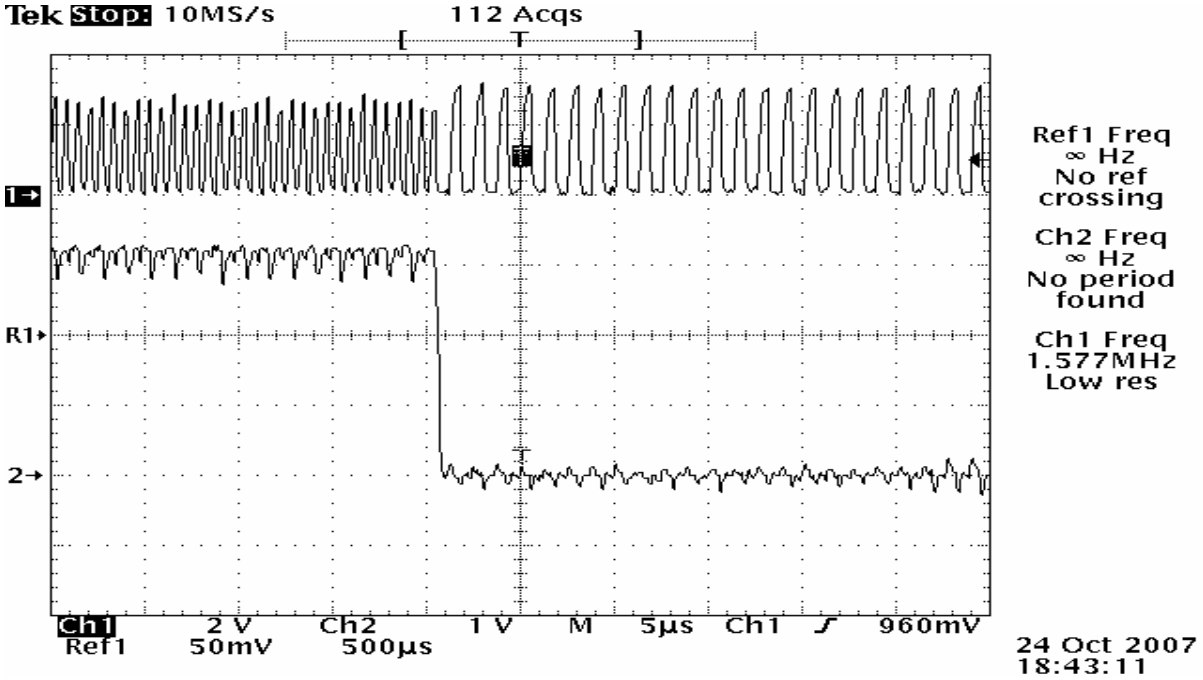


Fig. 4.32 Test result of high and low carrier when V_{DD} is 3.0V and input current is 2uA

(Magnified Picture)

Table 4.1 Simulation Result of Data Frequency

Input Current (uA)	Frequency (MHz)
0.2	3.68
0.7	4.35
1	6.29
1.5	9.57
1.8	11.55
2	12.87

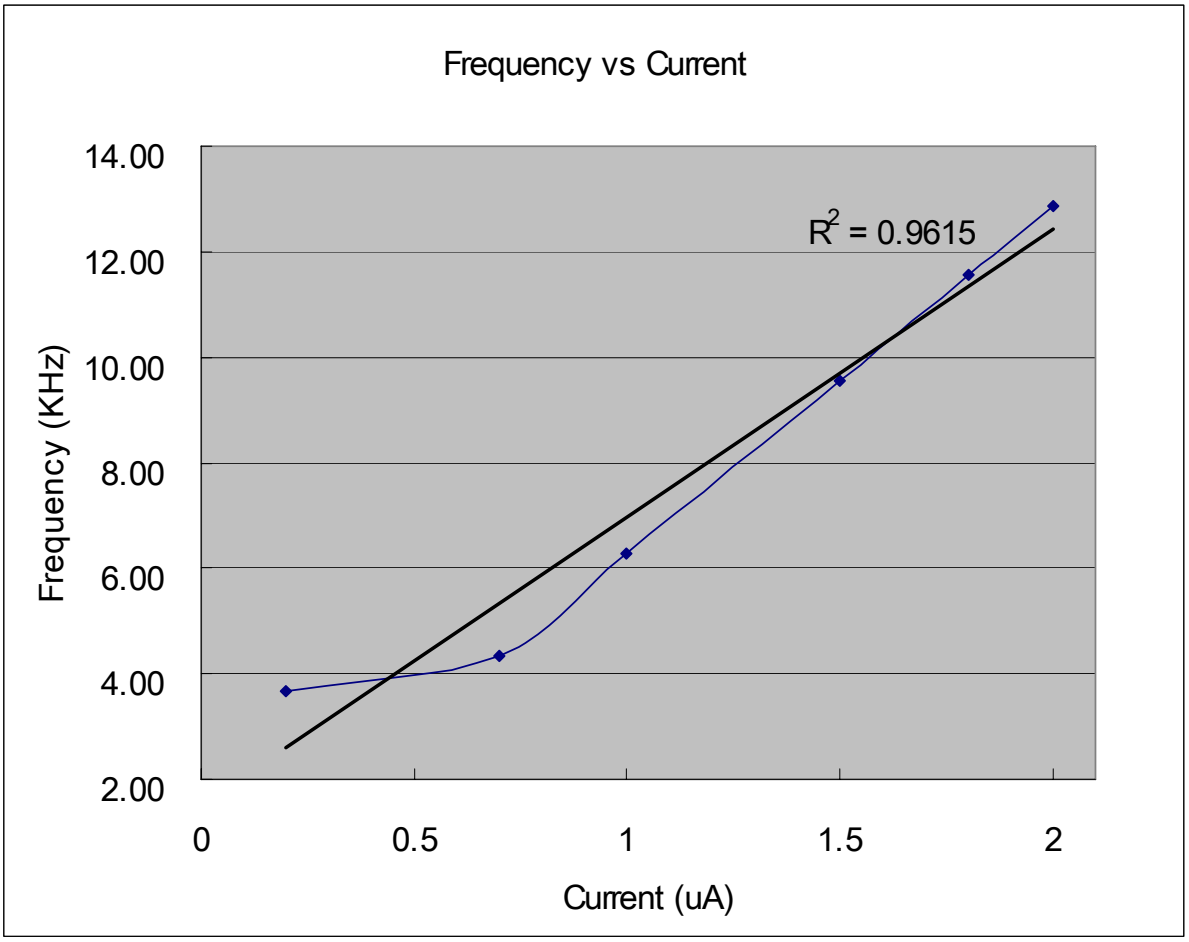


Fig. 4.33 Input current vs data frequency-Simulation

Table 4.2 Test Result of Data Frequency

Input Current (uA)	Frequency (MHz)
0.2	0.925
0.5	2.222
0.7	3.161
1	4.61
1.5	6.848
2	9.159

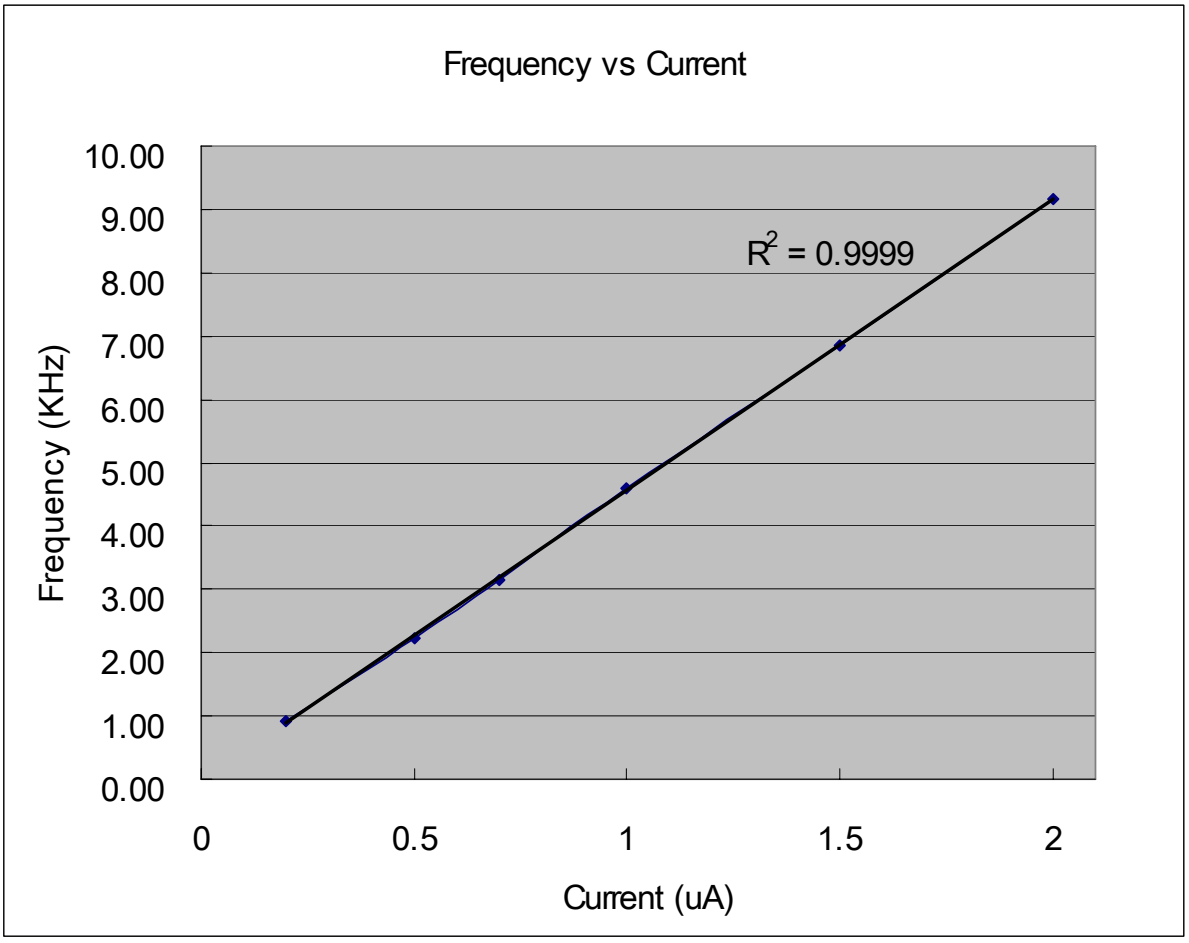


Fig. 4.34 Input current vs data frequency-Test

Fig. 4.14 through Fig.4.23 show the FSK, Data, High, and Low carrier frequency signals. Net63 is a data carrier signal, Net37 is a high carrier frequency, and Net31 is a low carrier frequency. Table 4.1 and 4.2 show the simulation and test result of data frequency. The data frequency range is little bit different from the test data because of the parasitic capacitances on the test board as well as in the probe. However, the linearity of the frequency is matched well. The low and high carrier frequencies are,

$$f_L = 514.8 \text{ KHz}$$

$$f_H = 1.029 \text{ MHz}$$

,and the measured low and high carrier frequencies are,

$$f_L = 786.2 \text{ KHz}$$

$$f_H = 1.65 \text{ MHz}$$

Unfortunately, these high and low carrier frequencies were not being correctly measured in 1.8V of supply voltage. The high carrier frequency can be measured correctly but because of interference of high carrier into low carrier, low carrier frequency varies a lot. Thus, the test results of high- and low- carrier frequencies are from the supply voltage of 3.0V, which shows the clear picture of carriers as well as both frequencies. In addition, the wave forms of high- and low-carrier frequencies are not correct. One reason for this could be the parasitic capacitance in the test board and the probe. When the chip is designed, unfortunately, these parasitic capacitances were not considered carefully. The other reason is that since the nominal operating

voltage of the AMI 0.5-µm CMOS process is 5V, and thus 1.8V has not been large enough to operate the circuit even though this circuit has been designed based on 1.8V of the power supply.

4.3.2 Bandgap and Voltage Regulator Simulation and Test Results

In this section, the simulation results of the bandgap as well as the voltage regulator have been presented. Fig. 35 and 36 show the DC sweep and temperature simulation results. Table 4.3 through 4.6 shows the results of the bandgap and the voltage regulator output voltage of before and after the load capacitor of 330pF is added

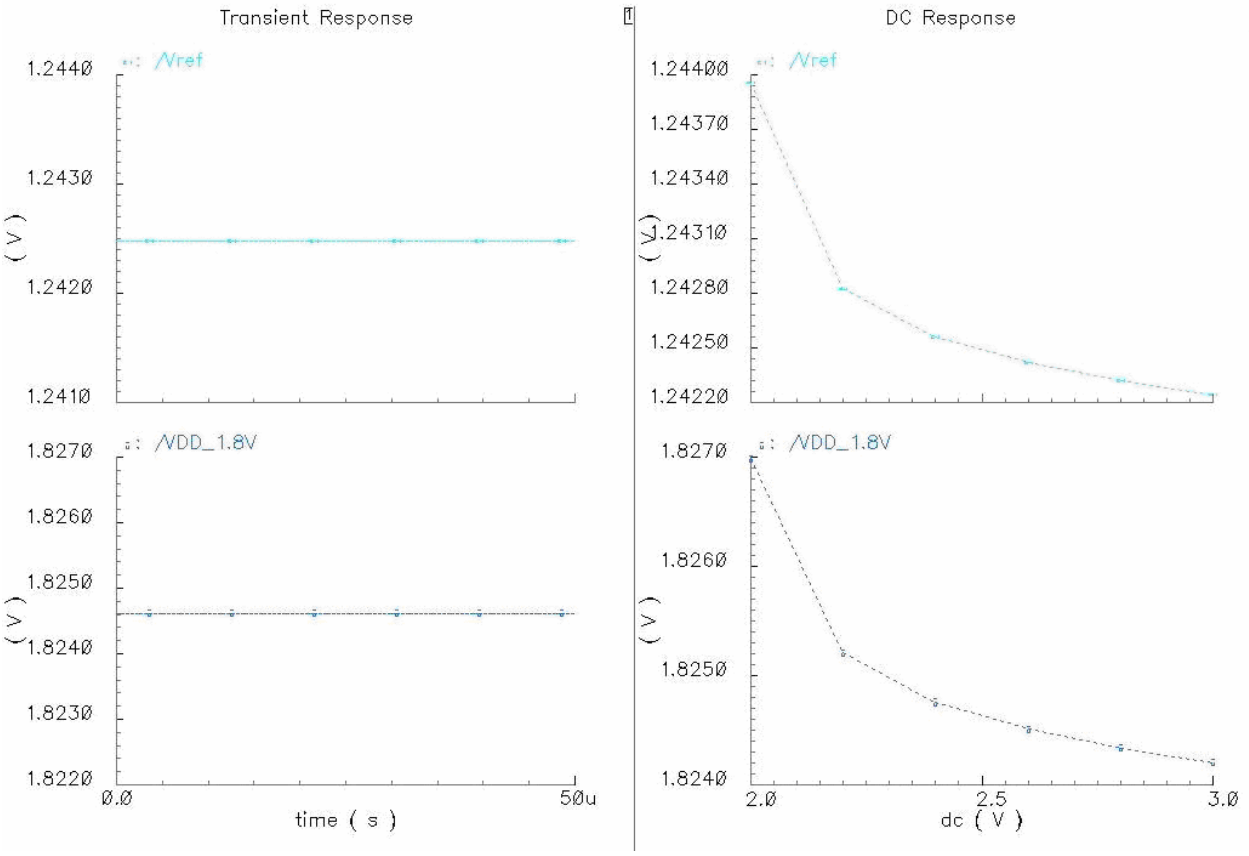


Fig. 4.35 The DC sweep simulation result of the bandgap reference and the voltage regulator

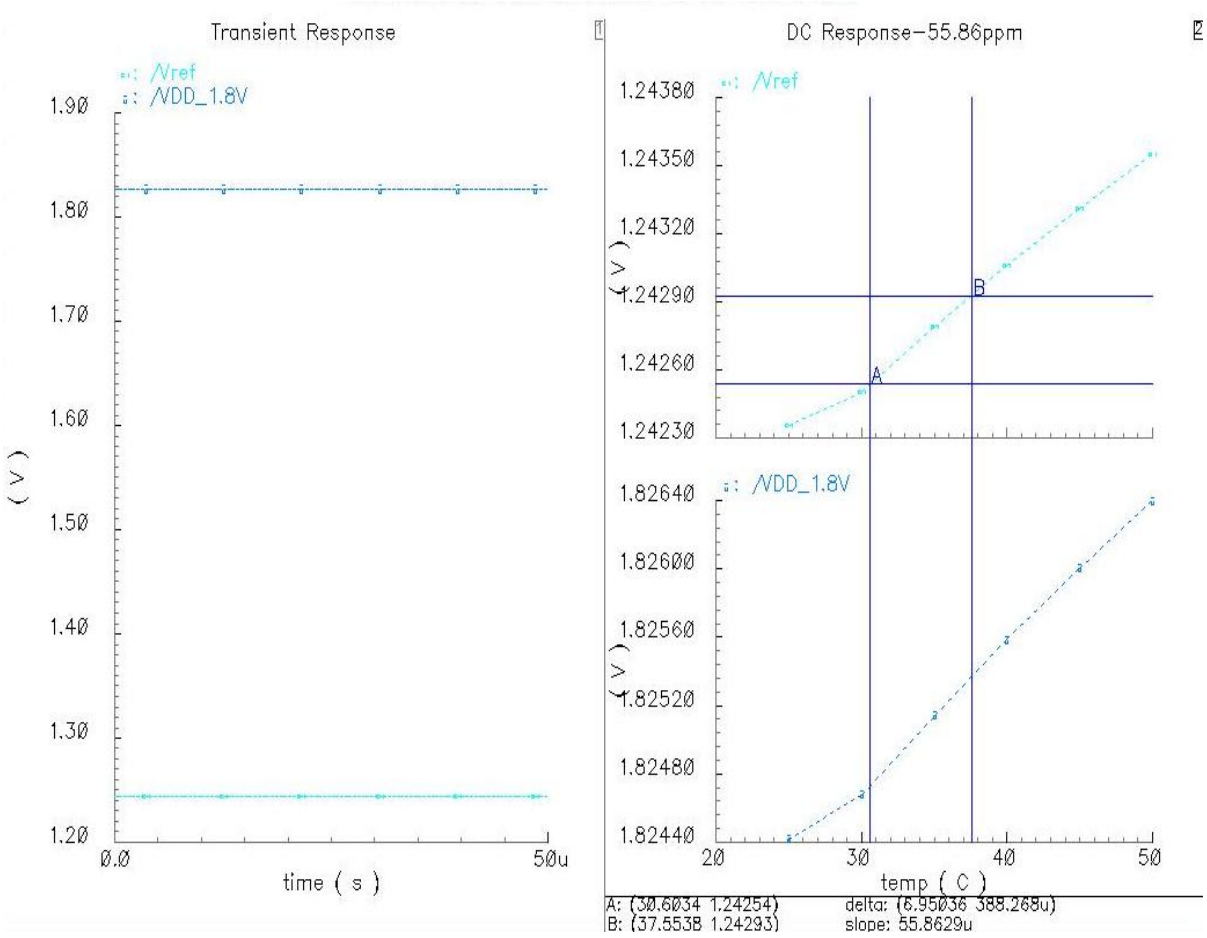


Fig. 4.36 Temperature simulation result of the bandgap reference and the voltage regulator

Table 4.3 Bandgap reference vs V_{DD} without load capacitance of 330pF

V_{DD} (V)	Bandgap Reference (V)
1.997	1.417
2.097	1.420
2.197	1.423
2.297	1.425
2.397	1.428
2.497	1.430
2.597	1.432
2.697	1.433
2.797	1.435
2.897	1.436
2.997	1.437

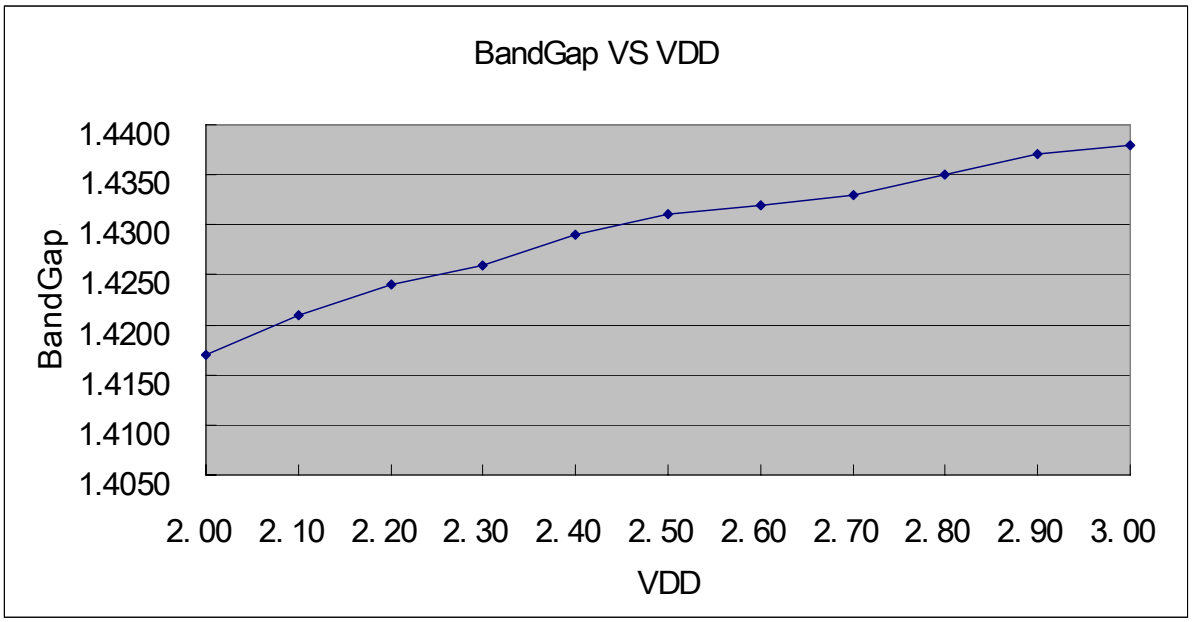


Fig. 4.37 Test results of the bandgap reference vs V_{DD}

Table 4.4 Voltage Regulator vs V_{DD} without load capacitance of 330pF

V_{DD} (V)	Voltage Regulator (V)
1.997	1.997
2.097	2.092
2.197	2.097
2.297	2.100
2.397	2.103
2.497	2.105
2.597	2.108
2.697	2.110
2.797	2.113
2.897	2.115
2.997	2.116

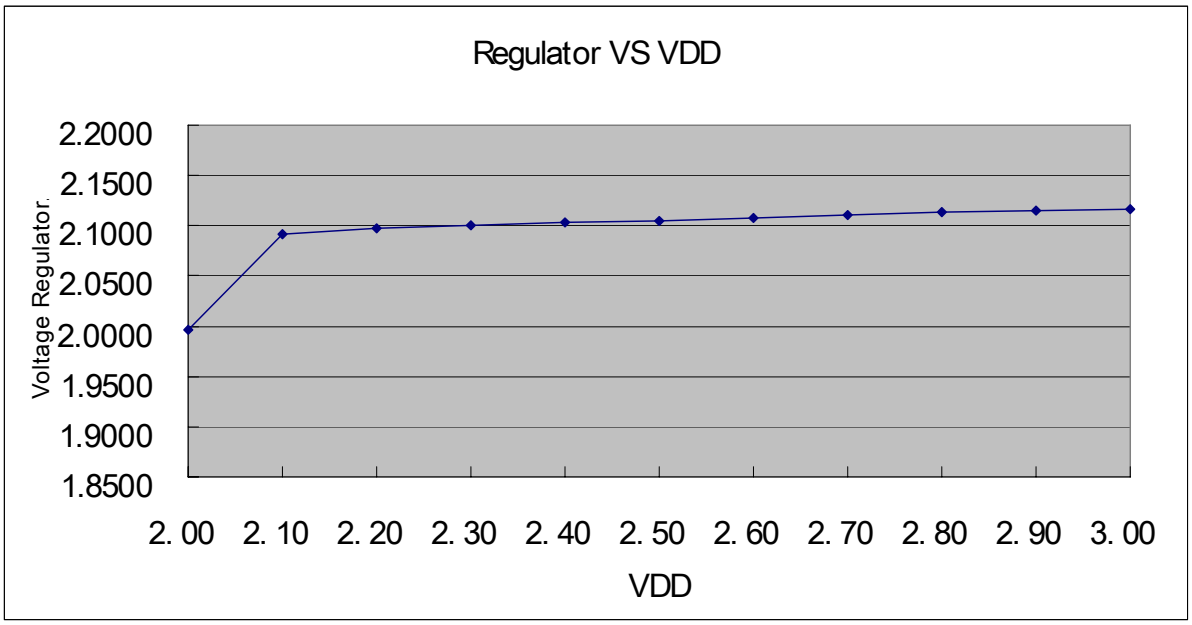


Fig. 4.38 Test results of voltage regulator vs V_{DD}

Table 4.5 Bandgap reference vs V_{DD} with load capacitance of 330pF

V_{DD} (V)	Bandgap Reference (V)
1.997	1.417
2.097	1.421
2.197	1.424
2.297	1.426
2.397	1.429
2.497	1.431
2.597	1.432
2.697	1.433
2.797	1.435
2.897	1.437
2.997	1.438

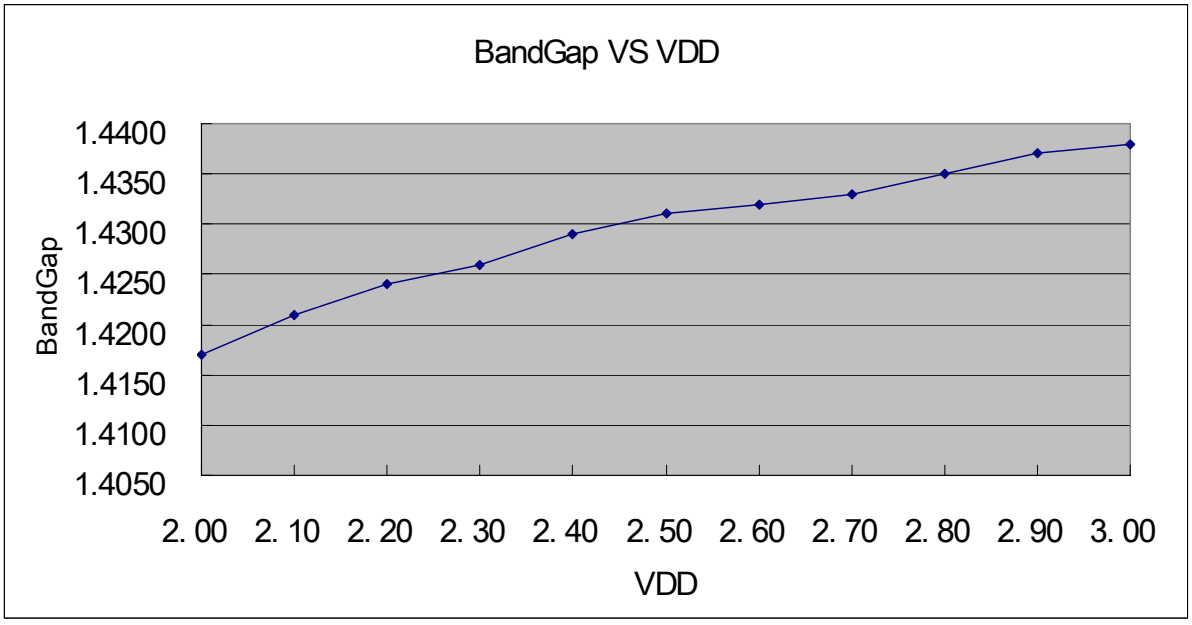


Fig. 4.39 Test results of the bandgap reference vs V_{DD}

Table 4.6 Voltage Regulator vs V_{DD} with load capacitance of 330pF

V_{DD} (V)	Voltage Regulator (V)
1.997	1.998
2.097	2.092
2.197	2.098
2.297	2.101
2.397	2.104
2.497	2.107
2.597	2.110
2.697	2.112
2.797	2.113
2.897	2.115
2.997	2.116

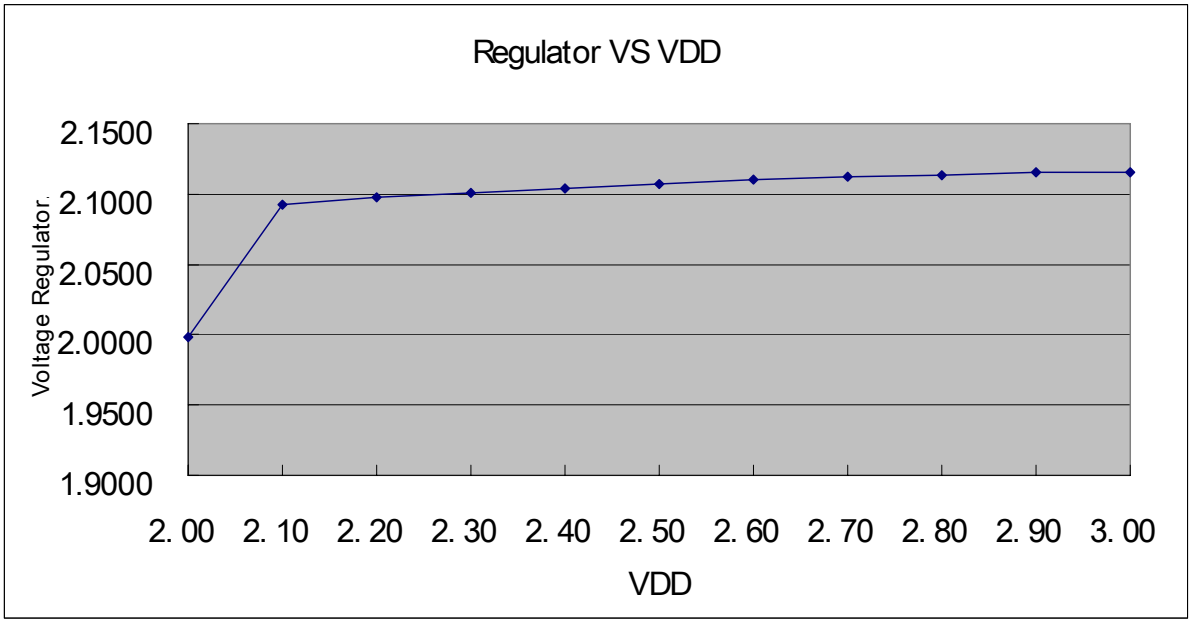


Fig. 4.40 Test results of voltage regulator vs V_{DD}

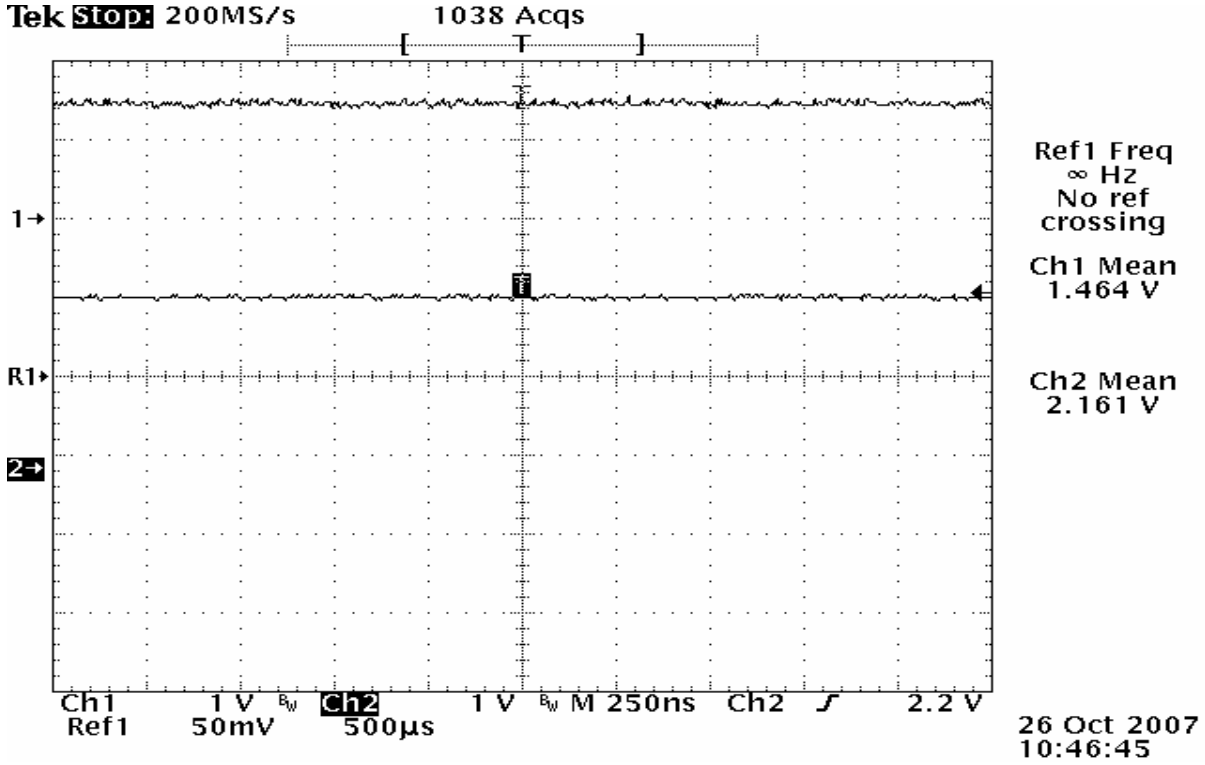


Fig. 4.41 Test results of voltage regulator and bandgap reference with load capacitance

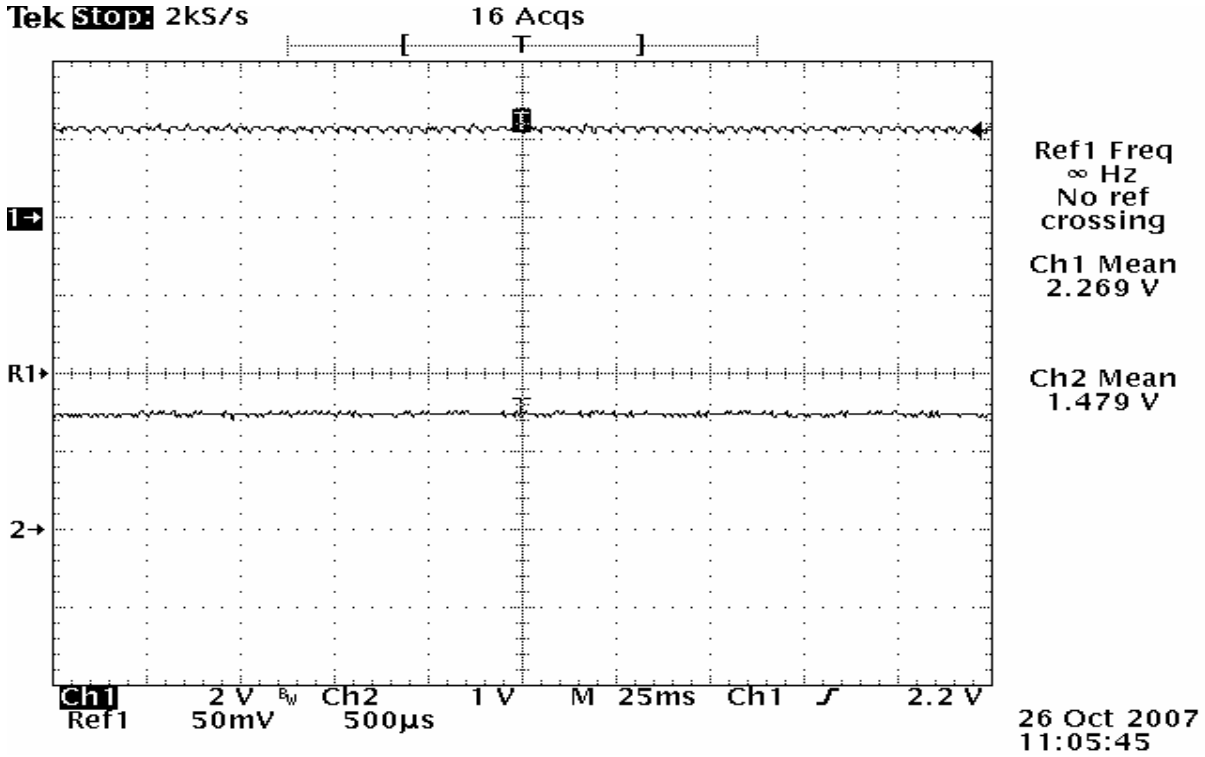


Fig. 4.42 Test results of voltage regulator and bandgap without load capacitance

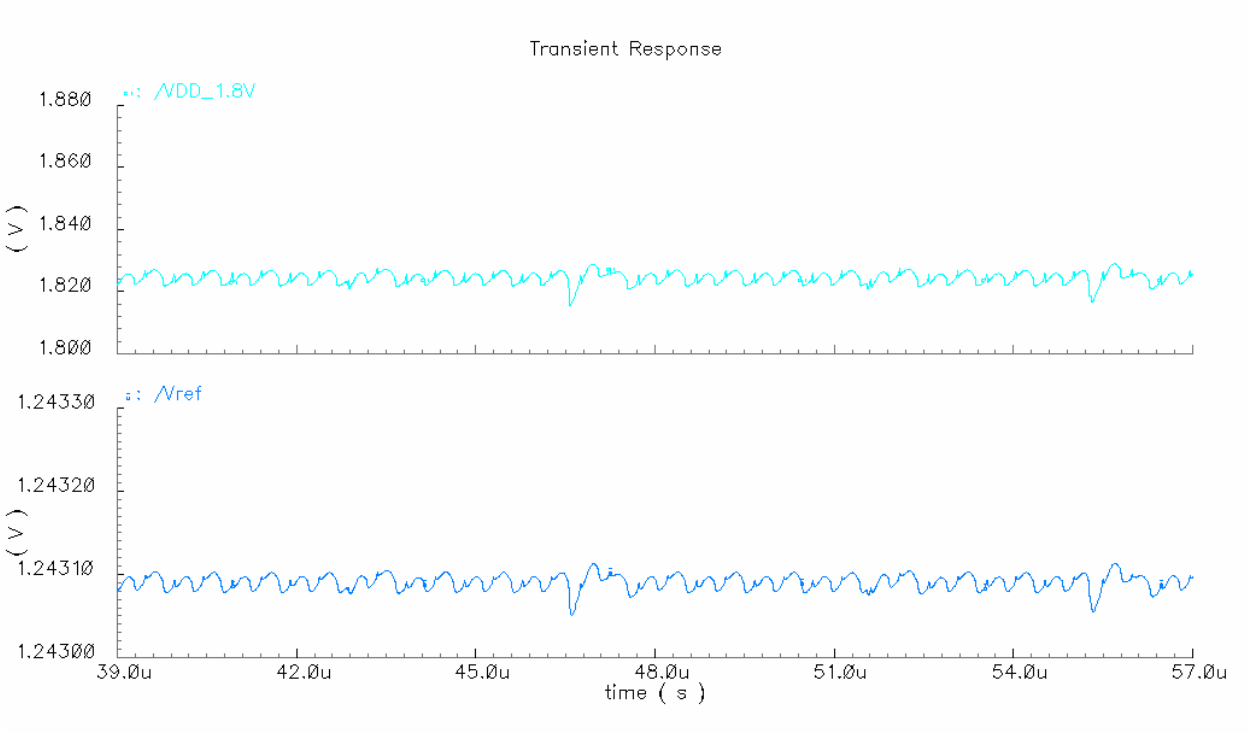


Fig. 4.43 Simulation results of voltage regulator and bandgap reference

Above figures and tables show the simulations and tests results of the bandgap reference and the voltage regulator outputs. In the simulation, the bandgap reference output voltage is 1.24 V approximately, and 1.82V for the voltage reference. A supply voltage for these two circuits is 2.5V. However, the test results show that the bandgap reference is 1.43V and voltage regulator is 2.1V approximately at 2.5V of supply voltage. The difference comes mostly from the process variation. Thus it can be concluded that the bandgap reference and the voltage regulator outputs are quite matched with each other.

With an external load capacitance of 330pF attached output of voltage regulator demonstrated better and smoother result compared to the case without the load capacitance. By looking at the simulation result, it can be seen that there are some rings in the output of both the bandgap reference as well as the voltage regulator. Also, in the test result in Fig. 4.44 shows some rings. However, after the load capacitance attached at the output of voltage regulator, the ringing disappears. Fig. 4.42, and Fig.4.43 show the results of the output of the bandgap reference and voltage regulator before and after the load capacitances are attached.

The temperature performance simulation of the bandgap reference circuit is shows in Fig. 4.37, and the DC Sweep is shown in Fig 4.36. The results of the temperature performance is 55.86 ppm/^{0}C , which is fairly good number for the bandgap temperature performance. The DC-Sweep performance is quite matched with the test data except the output voltage of both the bandgap reference and the voltage regulator circuits.

To improve the performance of both the bandgap and the voltage regulator, a higher gain from the operational amplifier is needed since this Op-Amp controls the difference from these both circuits.

4.3.3 Potentiostat

Fig. 4.45 shows the test result of the potentiostat. The input of $V_{ref\_Potentiostat}$, which is a positive input of U4 in Fig. 3.25. is 0.73V, and the output between R1 and R2 in Fig. 3.25. R1 is located in between the *work_electrode* and *reference_electrode*, and R2 is located in between the

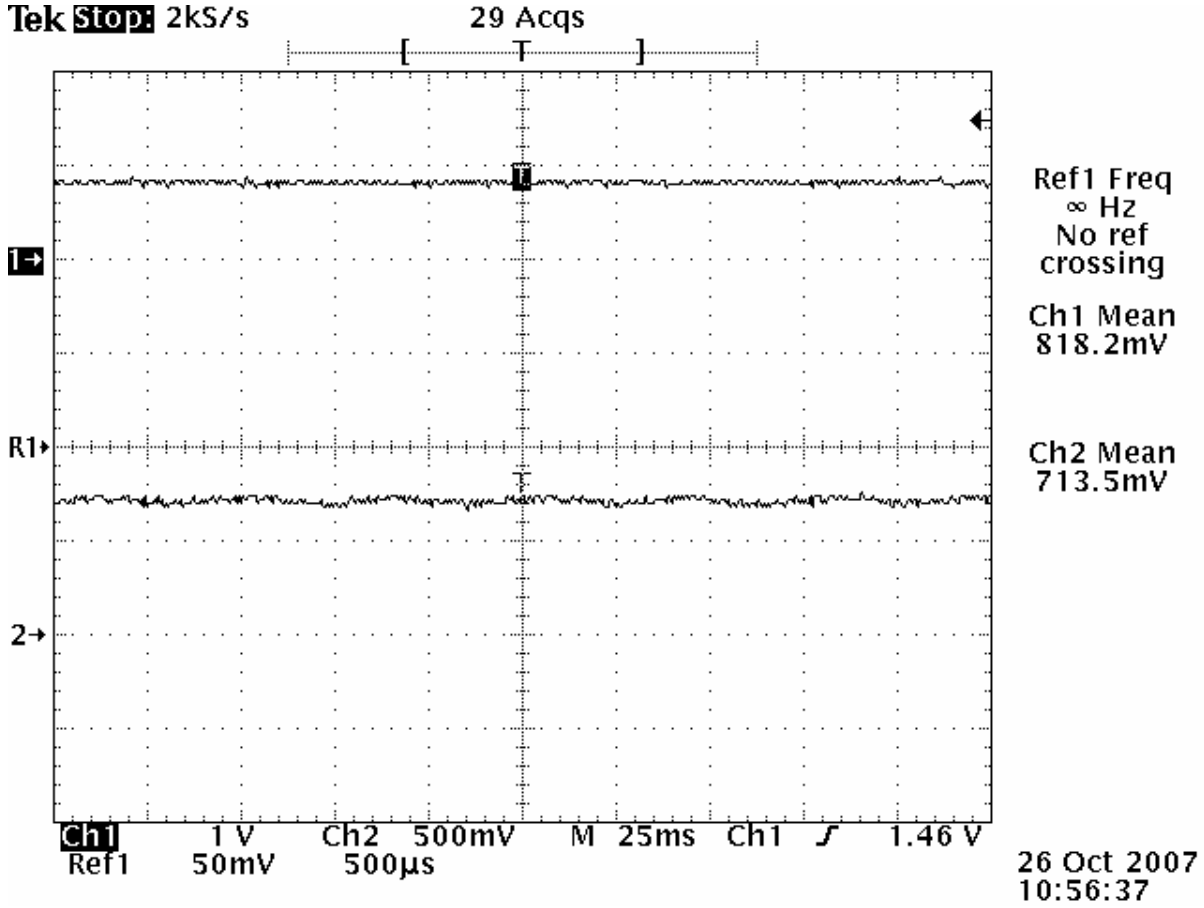


Fig. 4.44 Test results of the potentiostat

reference_electrode and *collect_electrode*. According to the requirement, as long as the voltage between the *work_electrode* and the *reference_electrode* maintain 0.7V, the *collect_electrode* will produce the current by chemical reaction. From the test result, it is easy to see that the requirement is fulfilled.

4.3.4 Power Consumption

The total current consumed by the entire chip in the simulation is about 494uA, and the external power supply voltage is 2.5V. So, the total power consumed by the chip is $1.24mW$. The tested value of total current is approximately 670uA and the total power consumed by the chip is$1.68mW$ with an external power supply of 2.5V, which is little higher than the simulated results. Most of the current is consumed by the potentiostat circuit since it contains four buffered operational amplifier to drive resistive load, which consumes a lot of current.

Chapter 5

Conclusion

5.1 Summary and Future Work

Compared to the simulation results of the entire chip, the actual data collected from the fabricated chip fulfills most of the requirements. However, carrier frequency generator of the signal processing part does not work as it is expected. The reasons that can be draw from the test data are,

1. The AMI 0.5-μm CMOS process is for the 5V technology. But the design, in the point of challenge, is based on the supply voltage of 2.5V for the bandgap, the voltage reference, and the potentiostat. The supply voltage for the signal processing part is even lower than 2.5V; that is 1.8V as a main power supply voltage. This low voltage causes reduced ability to drive the complete signal processing part.
2. During the layout, adequate number of connection for the power supply for the signal processing were not made. As a result, the power is not equally distributed throughout the entire signal processing block, and that causes some malfunction on digital parts inside the signal processing block. Also, the parasitic capacitance in the test board, and the probe should be carefully considered for the future work.

For the future work, high and low carrier frequency generator of the signal processing will need to be redesigned. Especially, the size of resistor, which is used to generate the fixed frequency, is required to be reduced in size. In addition, more careful layout of chip will need to be made for improved system performance.

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Appendix

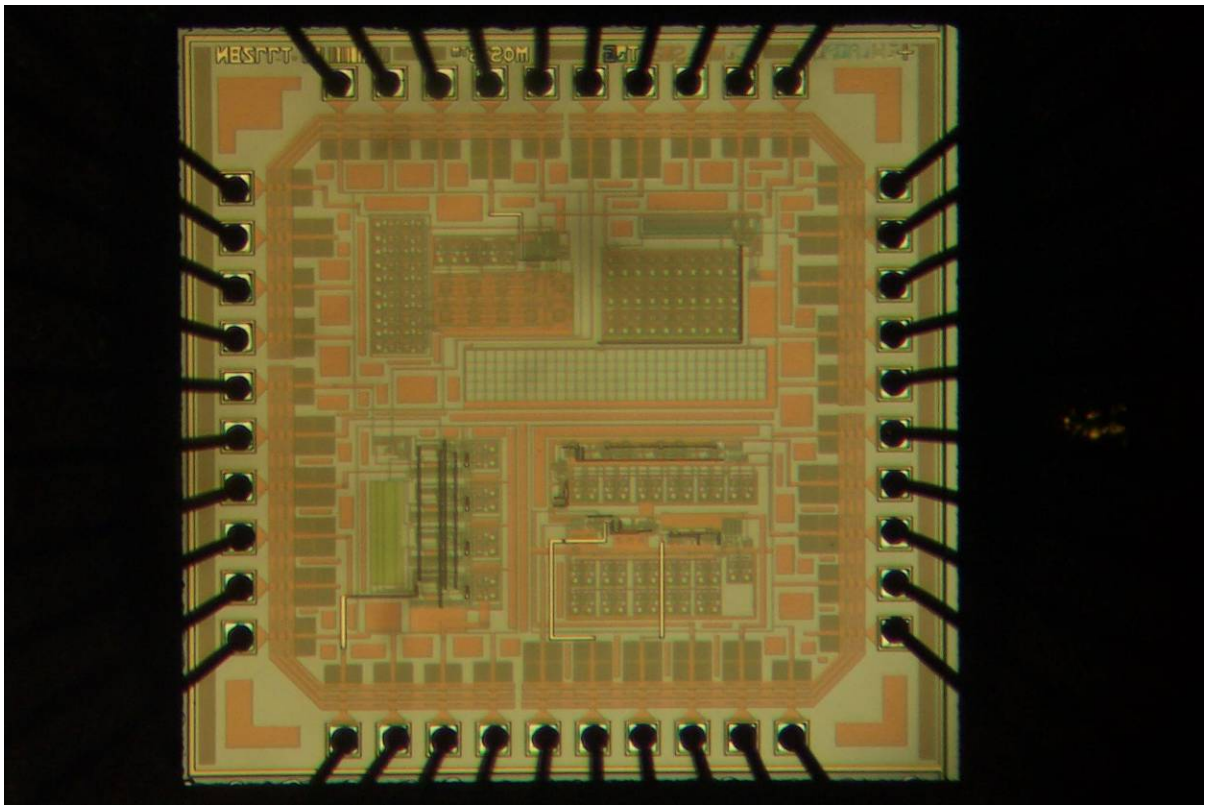

Fig.A.1 Actual chip

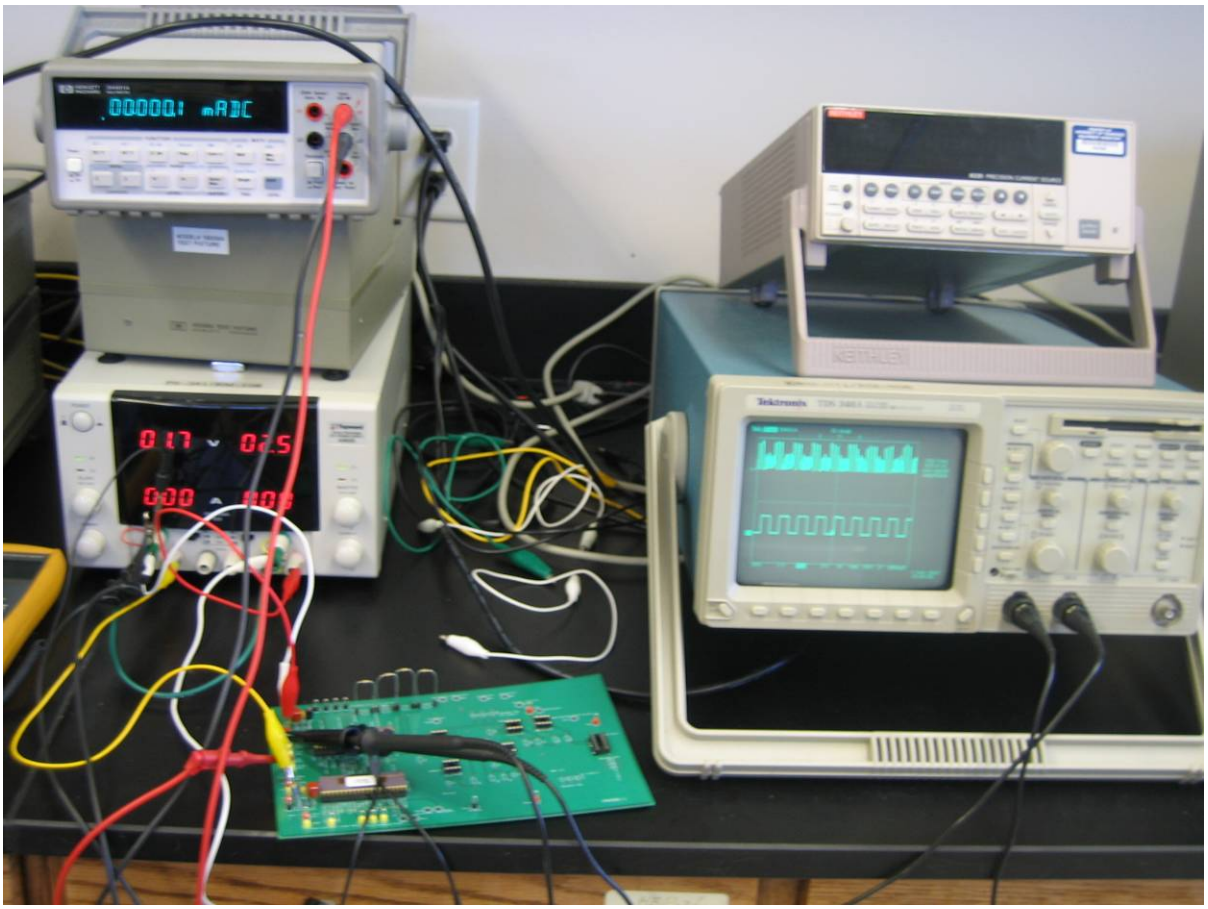

Fig.A.2 Test setup

Vita

Taeho Oh was born on December 11th, 1975 in Seoul, Korea. After he finished his schooling in Seoul, Korea in February 1994, he came to the United State of America in May 1994 to pursue his B.S degree.

He joined the University of Alabama in Huntsville majoring in Electrical and Computer Engineering in 1995. In 1999 Spring Semester, he started working as Co-Op engineer at Magnetek Inc. Madison, Alabama until 2000 summer. Year of 2000 summer, he graduated with a Bachelor of Science Degree in Electrical and Computer Engineering. After he served his army duty, he joined TRW Controls and Fasteners in Incheon, Korea in 2004.

Taeho has been working towards his Master's degree since January 2005 under the supervision of Dr.Syed Kamrul Islam, who is also his major advisor. His research focuses on CMOS-based analog/mixed-signal.